PIXELPLUS CO., LTD.

Preliminary Data sheet

PO2030N
1/4.5 Inch VGA Single Chip CMOS IMAGE SENSOR

[Preliminary]

Rev 0.29

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CMOS Image Sensor with 640 X 480 Pixel Array and Integrated On-Chip Image Signal Processor

Revision History

Version	Date [D/M/Y]	Notes	Writer
0.0	09/02/2004	*(Preliminary)* Features, Chip Arch, Frame Structure, Windowing, Still, Data Timing, I2C register edited	Hangkyoo Kim
0.1	10/02/2004	Register Descriptions	JongHo Shin
0.11	11/02/2004	Added the application note Modified reigster descriptions	SungJe Cheon
0.12	20/02/2004	Added Specifications	DS Min
0.13	20/02/2004	Modified application note	SungJe Cheon
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0.18	14/04/2004	Modified Default Register Value(Reg Addr 50h, 7Bh, 81h)	Bongju Lee
0.19	03/05/2004	Modified standby pin description and standby method Modified initialization registers in application note	SungJe Cheon
0.20	04/05/2004	Added AWB min/max register description	SungJe Cheon
0.21	02/06/2004	Modified Frame Width and Height description(Page 20, 21) And Tgcontrol1 description(Page 27)	BongJu Lee
0.22	05/06/2004	Modified Power consumption(Table 1)	BongJu Lee
0.23	28/07/2004	Modified supply voltage	SungJe Cheon
0.24	01/10/2004	Modified AC Characteristic	SungJe Cheon
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0.27	08/09/2005	Modified the application note	SungJe Cheon
0.28	26/09/2005	Modified I_{IN} parameter	BJ Lee

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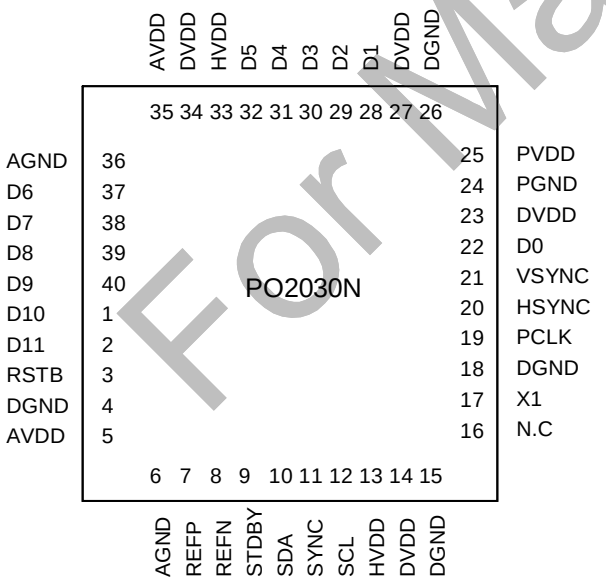
§ This document is an initial draft. It will be revised on without prior notice.
Contact Pixelplus for up-to-date information.

Features

- 1/4.5 inch 640 X 480 active pixel array with color filters and micro-lens.
- Power supply 2.5V for core and 2.5 ~ 2.8V (Max. 3.1V) for I/O.
- Output formats : 8bit YCbCr / 9Bit Bayer data / 5:6:5 RGB, 12bit 8:8:8 RGB / 8bit Y
- 30 frames/sec progressive scan @27 MHz master clock.
- Image processing on chip : lens shading, gamma correction, defect correction, low pass filter, color interpolation, edge enhancement, color correction, contrast stretch, color saturation, white balance, exposure control and back light compensation.
- Still image capture with electrical or mechanical shutter.
- Frame size, window size and position controllable through a serial interface bus.
- VGA / QVGA / QQVGA Scaling.
- Horizontal / Vertical mirroring.
- 50Hz, 60Hz flicker cancellation.
- Package : 40 pin CLCC, 32 pin CSP



< Figure. 1> Pin Diagram

Table 1. Typical Parameters

Pixel Array	648 X 488
Pixel Size	5.2um X 5.2um
Image Area	3.37mm X 2.54mm
Clock Rate	27MHz (Max.)
Frame rate	Variable up to 30fps
Dark Current	0.3 nA/㎠
Sensitivity	5V/Lux.sec @15fps,IR cut filter
Saturation Level	770 mV
Conversion Gain	15~50 ㎶/electrons
Fill Factor	40 %
Supply voltage	2.5~2.8V I/O,2.5V Core
Power consumption	80 mW @30fps, active
	30 uW @standby
Operation Temp.	-30 ~ 40℃
Dynamic Range	68 dB
Package	40 pin CLCC, 32 pin CSP

PIN Descriptions

Pin No.	Name	I/O Type	Functions / Descriptions
1	D10	O	Bit 10 of data output. Luminance data Y<7:0> are mapped to output pins D<11:4>. Chrominance data UV<7:0> are also mapped to output pins D<11:4>. Bayer RGB data are mapped to output pins D<11:3>.
2	D11	O	Bit 11 of data output.
3	RSTB	I	System reset must remain low for at least 8 master clocks after power is stabilized. When the sensor is reset, all registers are set to their default values.
4	DGND	P	Digital ground. Core and I/O circuits share the ground pads.
5	AVDD	P	Analog vdd : 2.5V DC. 100nF capacitor to AGND.
6	AGND	P	Analog ground.
7	CREF_P	O	ADC reference voltage. 100nF capacitor to AGND. ADC assumes V(REFP) – V(REFN) is the minimum input voltage that will be converted to 1FFh.
8	CREF_N	O	ADC reference voltage. 100nF capacitor to AGND.
9	STDBY	I	Power standby mode. When STDBY='1' there's no current flow in any analog circuit branch, neither any beat of digital clock. D<11:0> and PCLK, HSYNC, VSYNC pins can be programmed to tri-state or all '1' or all '0'. MCLK must be fixed to '1' or '0' after STDBY is set to '1' to avoid the leakage current. All registers retain their current values.
10	SDA	I/O	I2C serial data bus.
11	SYNC	O	Mechanical Shutter Close command Output.
12	SCL	I	I2C serial clock input.
13	HVDD	P	Digital vdd for I/O : DC 2.5~3.1V. Voltage range for all output signals is 0V ~ HVDD.
14	DVDD	P	Digital vdd for core logic : 2.5V DC. 100nF capacitor to DGND.
15	DGND	P	Digital ground for core and I/O circuits.
16	N.C	-	No Connection
17	X1	I	Master clock : Crystal input pad.
18	DGND	P	Digital ground.

Table 2-1. PIN Descriptions

Pin No.	Name	I/O Type	Functions / Descriptions
19	PCLK	O	Pixel clock. Data can be latched by external devices at the rising or falling edge of PCLK. The polarity can be controlled anyway.
20	HSYNC	O	Horizontal synchronization pulse. HSYNC is high (or low) for the horizontal window of interest. It can be programmed to appear or not outside the vertical window of interest.
21	VSYNC	O	Vertical sync : Indicates the start of a new frame.
22	D0	O	Bit 0 of data output.
23	DVDD	P	Digital vdd : 2.5V DC. 100nF to DGND
24	PGND	P	Ground for pixel array.
25	PVDD	P	Pixel array current is supplied from PVDD : 2.5V DC. 100nF to AGND
26	DGND	P	Digital ground.
27	DVDD	P	Digital vdd : 2.5V DC. 100nF to DGND
28	D1	O	Bit 1 of data output.
29	D2	O	Bit 2 of data output.
30	D3	O	Bit 3 of data output.
31	D4	O	Bit 4 of data output.
32	D5	O	Bit 5 of data output.
33	HVDD	P	Vdd for I/O : 2.5~3.1V
34	DVDD	P	Digital vdd : 2.5V DC. 100nF to DGND
35	AVDD	P	Analog vdd : 2.5V DC, 100nF to AGND
36	AGND	P	Analog ground.
37	D6	O	Bit 6 of data output.
38	D7	O	Bit 7 of data output.
39	D8	O	Bit 8 of data output.
40	D9	O	Bit 9 of data output.

Table 2-2. PIN Description

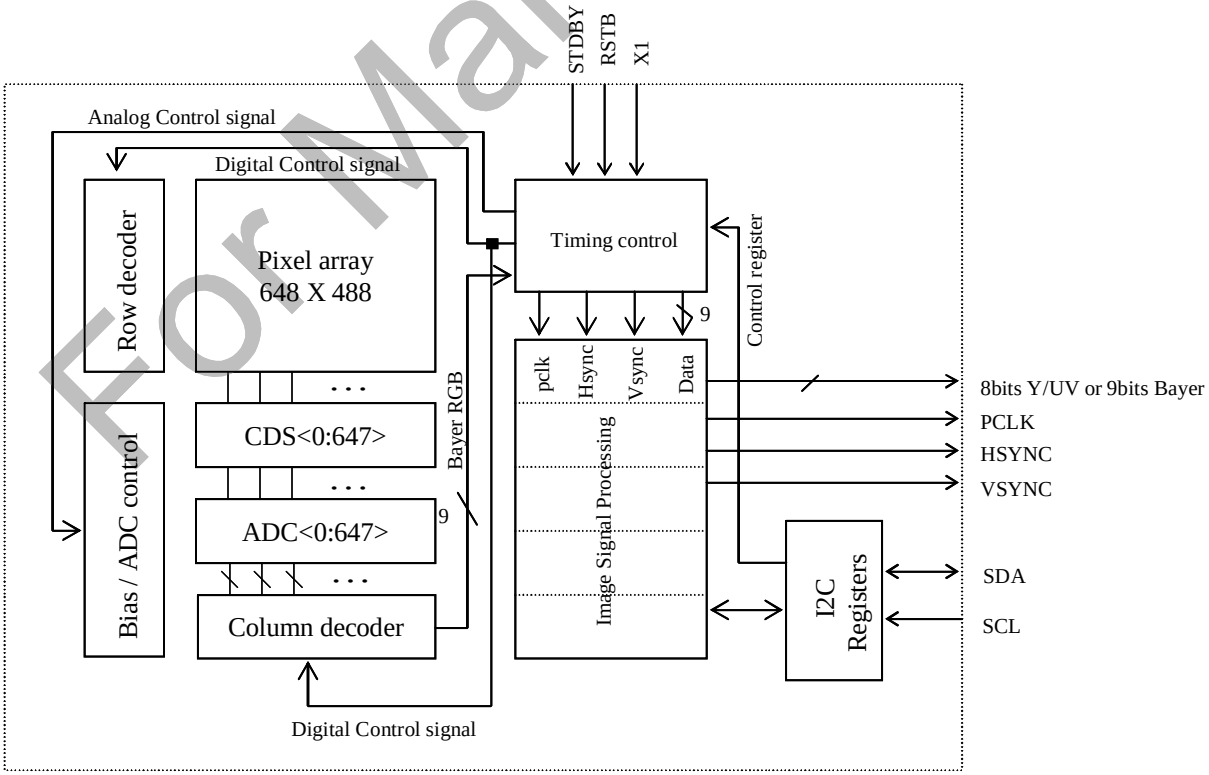
CMOS Image Sensor with 640 X 480 Pixel Array and Integrated On-Chip Image Signal Processor

Signal Environment

PO2030N has 2.8V tolerant Input pads. Input signals must be higher than or equal to HVDD but cannot be higher than 2.8V. PO2030N input pad has built in reverse current protection circuit, which makes it possible to apply input voltage even if the HVDD is disconnected or floating. Voltage range for all output signals is 0V ~ HVDD.

Chip Architecture

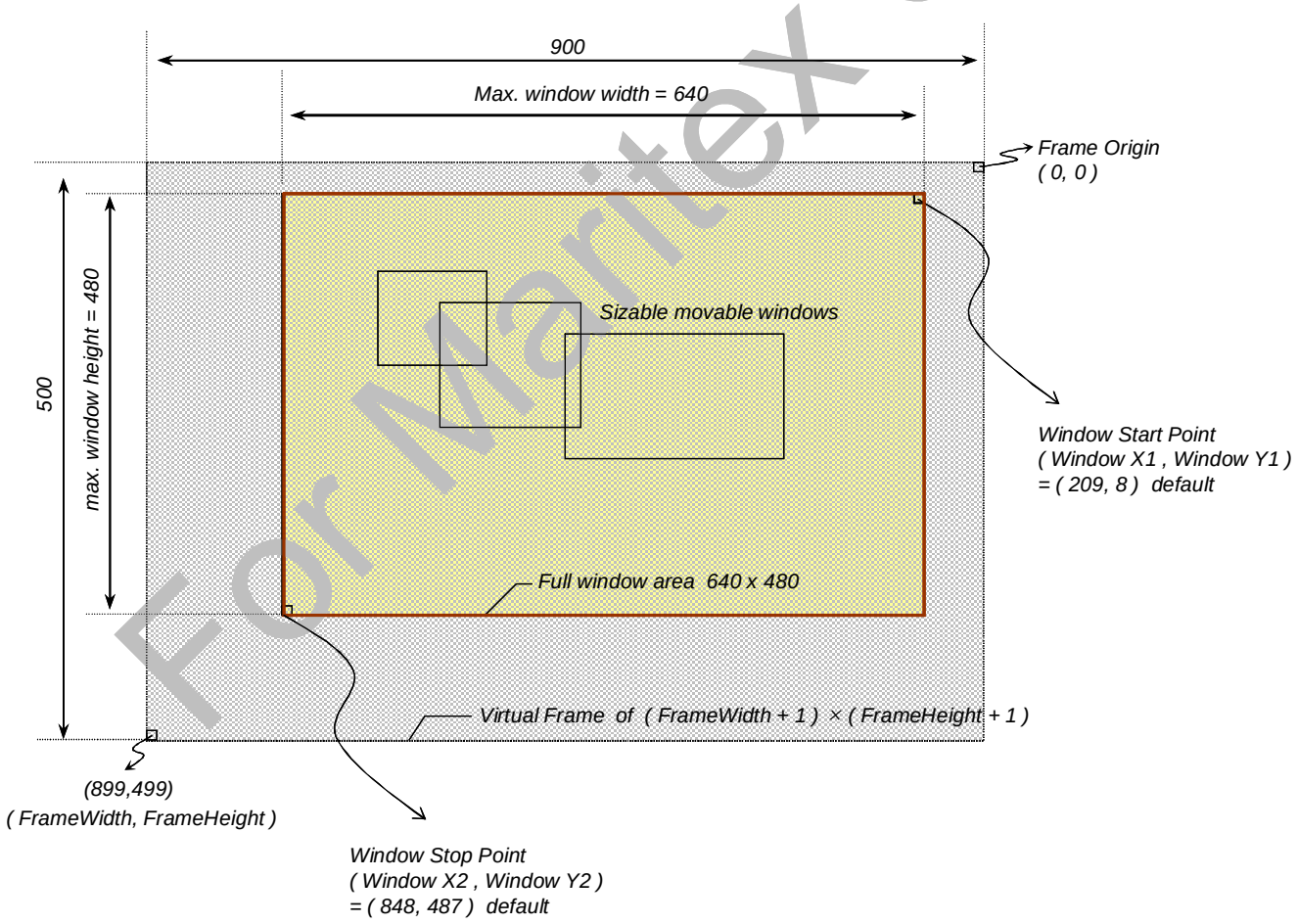
PO2030N has 648 x 488 effective pixel array and column/row driver circuits to read out the pixel data progressively. CDS circuit reduces noise signals generated from various sources mainly resulting from process variations. Pixel output is compared with the reset level of its own and only the difference signal is sampled, thus reducing fixed error signal level. Each of R, G, B pixel output can be multiplied by different gain factors to balance the color of images in various light conditions. The analog signals are converted to digital forms one line at a time and 1 line data are streamed out column by column. The Bayer RGB data are passed through a sequence of image signal processing blocks to finally produce YCbCr 4:2:2 output data. Image signal processing includes such operations as gamma correction, defect correction, low pass filter, color interpolation, edge enhancement, color correction, contrast stretch, color saturation, white balance, exposure control and back light compensation. Internal functions and output signal timing can be programmed simply by modifying the register files through I^2C serial interface.



<Figure. 2> Block Diagram

Frame Structure and Windowing

Origin *(0, 0)* of the frame is at the upper right corner. Size of the frame is determined by two registers : *FrameWidth* and *FrameHeight.* One frame consists of *FrameWidth + 1* columns and *FrameHeight + 1* rows. *FrameWidth* and *FrameHeight* can be programmed to be larger than physical array size. Physical array of 640 × 480 pixels is positioned at *(209, 8).* It is possible to define a specific region of the frame as a window. Pixel scanning begins from *(0, 0)* and proceeds row by row downward, and for each line scan direction is from right to the left. HSYNC signal indicates if the output is from a pixel that belongs to the window or not. There are two counters to indicate the present coordinate of frame scanning : Frame row counter and frame column counter. Counter values repeat the cycle of 0 to *FrameHeight* , and 0 to *FrameWidth* respectively. The counter values increase at the pace of pixel clock (PCLK), which does not change as the frame size is altered. (ref. reg87h ~ 8Ch) The pixel data rate is fixed and is independent of frame size (frame rate.)



< Fig. 3 > Default structure of frame and window. (Top view)

Data Formats

Pixel array is covered by Bayer color filters as can be seen in the figure below. Since each pixel can have only one type of filter on it, only one color component can be produced by a pixel. PO2030N provides this Bayer pattern RGB data through an 9bit channel. But since it is necessary to know all 3 color components R, G, B to produce a color for a pixel, the other two components must be inferred from other pixel data. For example, G component for a B pixel is calculated as an average of its four nearest G neighbors, and its R component as an average of its four nearest R neighbors. This operation of inferring missing data from existing ones is called the color interpolation. Color interpolation produces an undesirable artifact in image. Sampling nature of color filter can leave an interference pattern around an area with repetitive fine lines. PO2030N adopts a low pass filter to prevent the interference patterns(called Moire pattern) from degrading the image quality too much. After color interpolation, every pixel has all three color components. These three color components R, G, B can be routed to 12 bit output pins in such a way that 8bit R data and upper 4bits of G data are passed first and then, lower 4 bits of G data and 8bit B data are passed to output pins. It takes two PCLK's to pass one pixel RGB data to output bus.

G1	R	G1	R
B	G2	B	G2
G1	R	G1	R
B	G2	B	G2

< Fig. 4> Bayer filter pattern

For low grade display devices, it is not necessary to have 3 RGB data of all 8bit precision. PO2030N provides lower precision RGB data such that, 5bit R data and upper 3 bits of 6bit precision G data are passed first to output pins, and then the remaining 3 bits of G and 5 bit B data are routed outward. It takes two PCLK's to get 5:6:5 RGB data for each pixel.

It is possible to extract monochrome luminance data from RGB color components and the conversion equation is : Y = 0.299R + 0.587G + 0.114B where R,G and B are gamma corrected color components. And the color information is separated from luminance information according to following equations.

$$U = 0.492 (B – Y)$$
$$V = 0.877 (R – Y)$$

Since human eyes are less sensitive to color variation than to luminance, color components can be sub-sampled to reduce the amount of data to be transmitted, but preserving almost the same image quality.

U1	Y1	V1	Y2	U3	Y3	V3	Y4	…

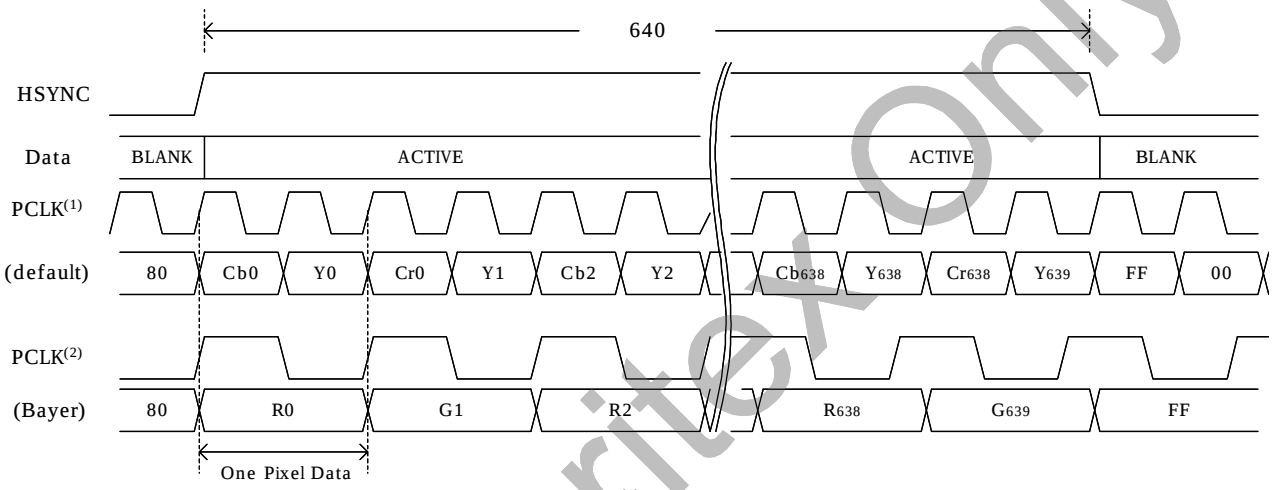
< Fig. 5> 4:2:2 YUV data sequence.

PO2030N supports 4:2:2 YUV data format where U and V components are horizontally sub-sampled such that U and V for every other pixel are omitted. PO2030N also supports ITU-R BT.601 YC_BC_R format which is a scaled, offset version of YUV. Y is the same in both formats but the C_BC_R is formed as follows.

$$C_B = 0.564 (B – Y) + 128$$
$$C_R = 0.713 (R – Y) + 128$$

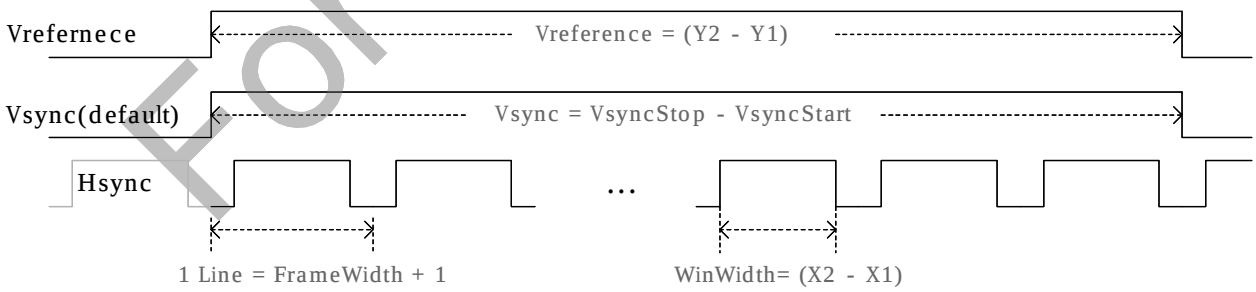
Data and Synchronization Timing

In <Fig.6>, HSYNC / VSYNC / PCLK polarity can have any combinations possible (Except for RGB Bayer). Data can be latched at the rising or falling edge of PCLK. HSYNC and VSYNC can be set to be active high or active low. Every type of data (RGB or YUV) comes out at the fixed rate of PCLK, which can have the same or ½ ~ 1/128 the frequency of MCLK. The sequence RGB Raw Bayer data for even rows is RGRGRG… and for odd rows is GBGBGB….



PCLK(1) : clk for YCbCr, RGB565, RGB888 data format
PCLK(2) : clk for Bayer, Mono data format

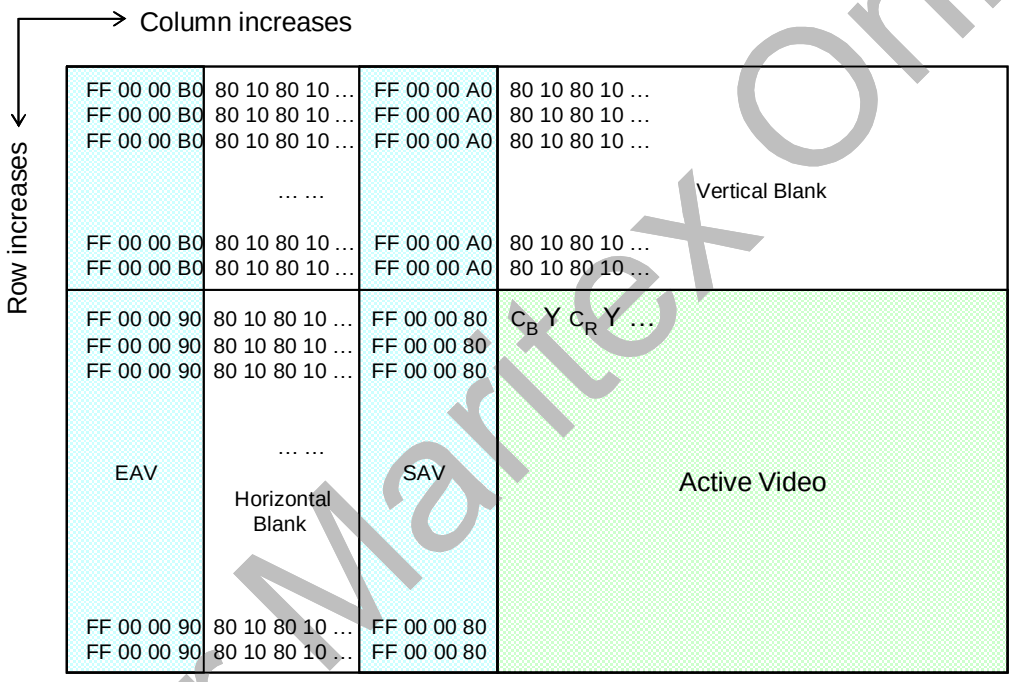
< Figure. 6 > Timing diagram for HSYNC, PCLK and data



< Figure. 7> Timing diagram for VSYNC and HSYNC

In <Fig.7>, The width of VSYNC/Vreference pulse can be controlled by VsyncStart/VsyncStop and WindowY1/Y2 registers : Vreference width = (WindowY2 - WindowY1), Vsync Width = (VsyncStop - VsyncStart).
The width of Hsync pulse can be controlled by windowX1/X2 registers: Hsync Width = WindowX2 - WindowX1 (ref. reg08h ~ 0Fh, reg87h ~8Ch descriptions)

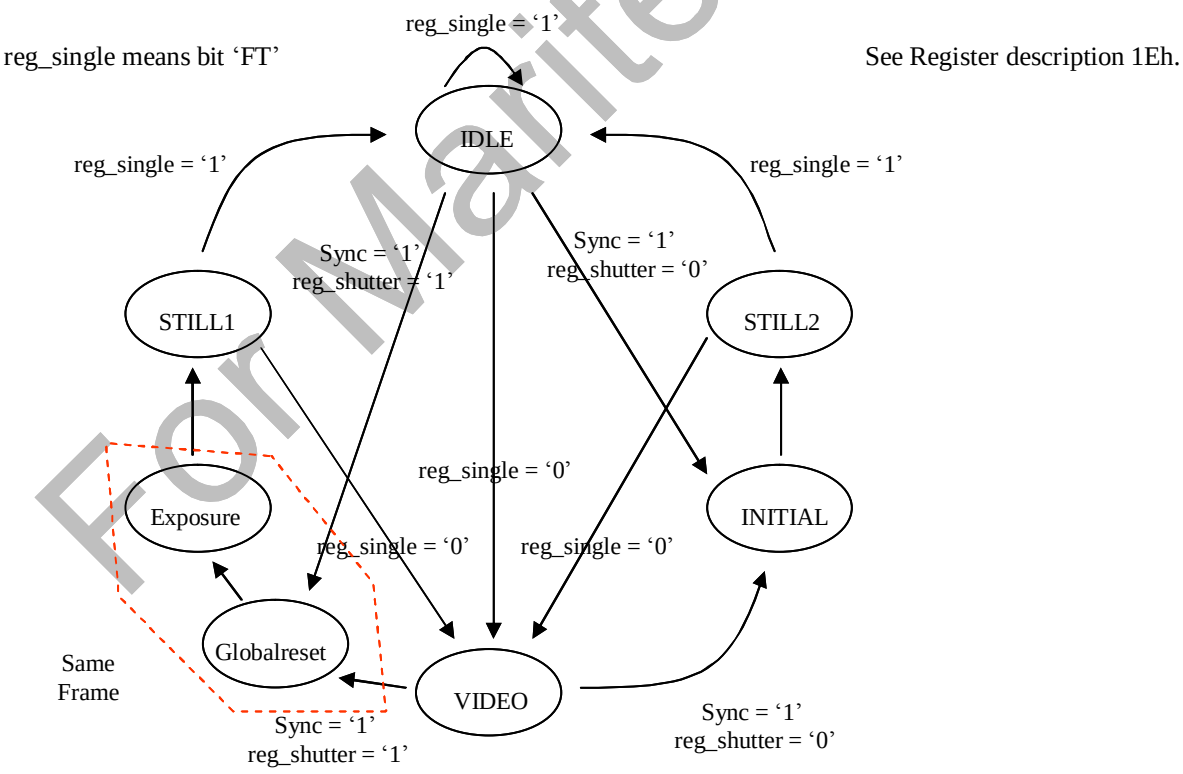
In <Fig. 8>, EAV(End of Active Video) and SAV(Start of Active Video) signals are inserted for synchronization purposes. EAV is a 4 byte sequence of "FF 00 00 90" for active lines, and "FF 00 00 B0" for blank lines. SAV is a 4 byte sequence of "FF 00 00 80" for active lines, and "FF 00 00 A0" for vertical blank lines. HSYNC signal is asserted right after the SAV sequence and de-asserted right before the EAV sequence. Horizontal and vertical blank area is repeatedly filled with "80 10".



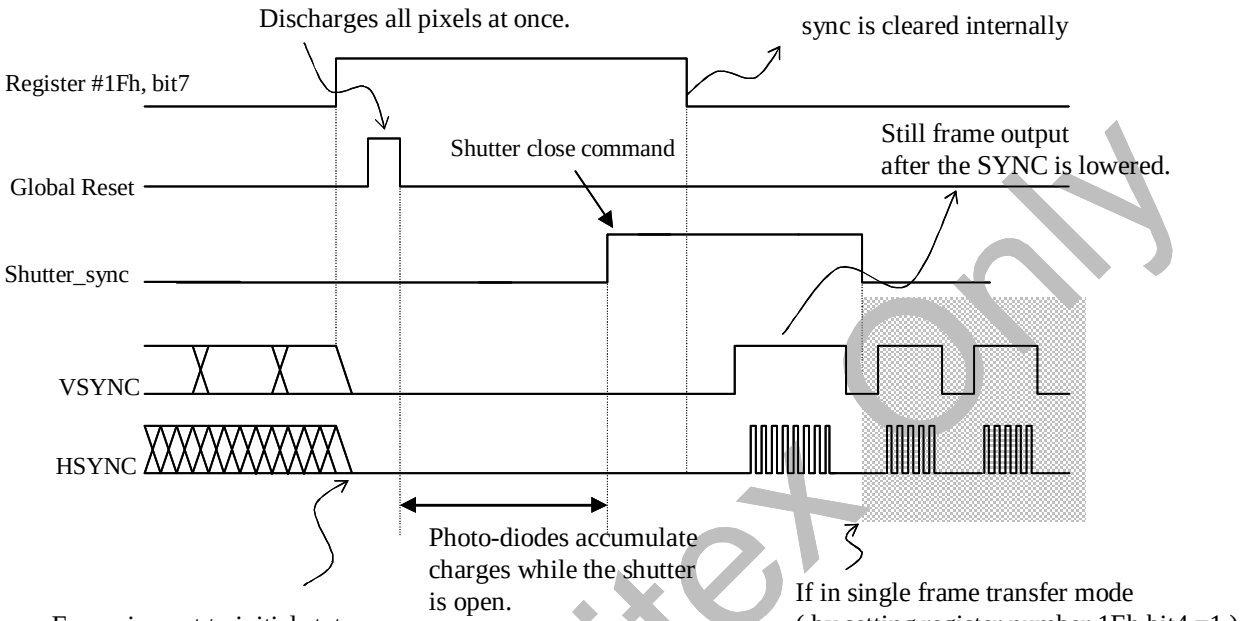
< Figure 8 > Frame data sequence including EAV and SAV.

Video Mode(Preview Mode) and Still Image Capture Mode

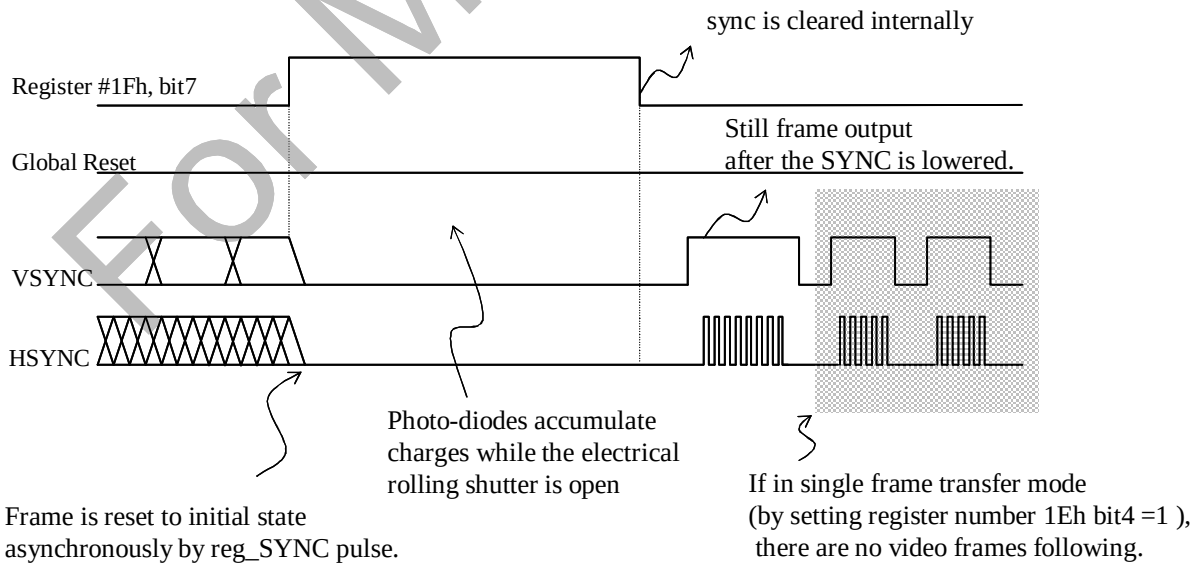
PO2030N normally operates in video mode. There are two kinds of still image capture mode. The first one is for a system that utilizes mechanical shutter (still1 mode). If there is a pulse on SYNC input (bit7 of register 1Fh), each and every pixel of the array is reset to dark state where there are no photo-charges accumulated (this is called GlobalReset state), and row/column counters are reset to initial states. While the SYNC is high, shutter is open and sensor is exposed to light. After the SYNC input goes low, there comes out the still image data. The other one (still2 mode) utilizes integrated electrical rolling shutter. After a still image capture mode, video mode may follow immediately, or the sensor may be in idle state until an appropriate bit(FT, bit4 of register 1Eh) is reset in the I^2C register file. While the sensor is in idle state, there's no HSYNC or VSYNC pulse. Image resolution switch between video and still mode (for example, video in QCIF resolution and still image in CIF resolution) can be done manually or automatically. Frame rate for the two modes can be always kept same. Exposure time can also be matched between the two modes of operation.



< Figure 9 > Sensor state transition diagram



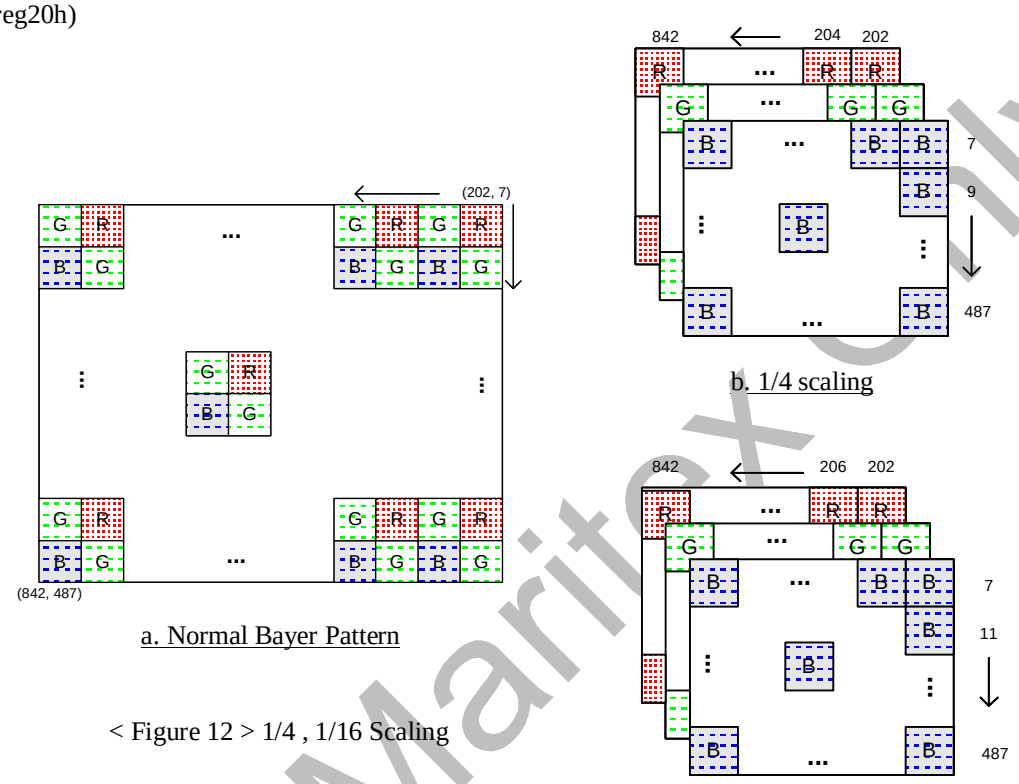
<Figure 10> Still image capture with mechanical shutter (register 1Eh bit5 = 1)



<Figure 11> Still image capture with electrical shutter (register 1Eh bit5 = '0')

Scaling

PO2030N supports four modes of scaling : 1/4 scaling, 1/16 scaling. Figure 12 shows the scaling four modes. (Ref. reg20h)



a. Normal Bayer Pattern

b. 1/4 scaling

c. 1/16 scaling

< Figure 12 > 1/4 , 1/16 Scaling

Exposure Time Control

IntLines<19:0> register controls the exposure time. *IntLines*<19:6> is the number of lines for which electrical shutter will be open to collect photons. *IntLines*<5:0> is the number of partial line times to be added to integer line numbers, which means the exposure time can be controlled by 1/64 line time. To guarantee same amount of exposure time between two different sampling modes, it is necessary to adjust some parameters. The parameters are : *IntLines*, *FrameWidth*, clock frequency, number of sampled data. For two different sampling modes A and B, the exposure time has a relation like

$$\text{exposure time(A)} = \frac{(\,\#\text{ of data(A)}\,) \times IntLines(\text{A}) \times FrameWidth(\text{A}) \times \text{clkfreq(B)}}{(\,\#\text{ of data(B)}\,) \times IntLines(\text{B}) \times FrameWidth(\text{B}) \times \text{clkfreq(A)}} \text{ exposure time(B)}$$

Suppose A is ¼ sampling mode and B is full sampling mode. The ratio of sample numbers is ¼ and lets assume the *IntLines* and *FrameWidth* register values are kept identical in both modes. If clock frequency is also fixed before and after the mode switch, the exposure time in mode A is ¼ that of mode B. To adjust the exposure level to be equal, mode A clock frequency can be slowed down by a factor of 1/4. Or the *IntLines* register value can be incremented four times while leaving other parameters same as mode B. Or the *FrameWidth* can be doubled while clock frequency is halved.

I2C Description

The registers of PO2030N are written and read through the I²C interface. The PO2030N has I²C slave. The PO2030N is controlled by the I²C clock (SCL), which is driven by the I²C master. Data is transferred into and out of the PO2030N through the I²C data (SDA) line. The SCL and SDA lines are pulled up to VDD by a 2kΩ off-chip resistor. Either the slave or master device can pull the lines down. The I²C protocol determines which device is allowed to pull the two lines down at any given time.

Start bit

The start bit is defined as a HIGH to LOW transition of the data line while the clock line is HIGH.

Stop bit

The stop bit is defined as a LOW to HIGH transition of the data line while the clock line is HIGH.

Slave Address

The 8-bit address of an I²C device consists of 7 bits of address and 1 bit of direction. A 0 in the LSB of the address indicates write mode, and a 1 indicates read-mode.

Data bit transfer

One data bit is transferred during each clock pulse. The I²C clock pulse is provided by the master. The data must be stable during the HIGH period of the I²C clock : it can only change when the I²C clock is LOW. Data is transferred 8 bits at a time, followed by an acknowledge bit.

Acknowledge bit

The receiver generates the acknowledge clock pulse. The transmitter (which is the master when writing, or the slave when reading) releases the data line, and receiver indicates an acknowledge bit by pulling the data line low during the acknowledge clock pulse.

No-acknowledge bit

The no-acknowledge bit is generated when the data line is not pulled down by the receiver during the acknowledge clock pulse. A no-acknowledge bit is used to terminate a read sequence.

Sequence

A typical read or write sequence begins by the master sending a start bit. After start bit, the master sends the slave device's 8-bit address. The last bit of the address determines if the request will be a read or a write, where a 0 indicates a write and a 1 indicates a read. The slave device acknowledges its address by sending an acknowledge bit back to the master.

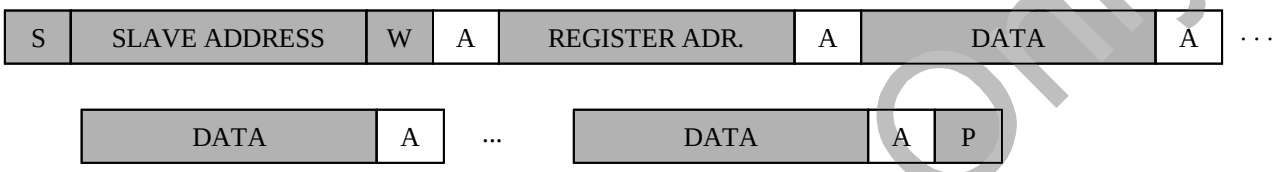
If the request was a write, the master then transfers the 8-bit register address to which a write should take place. The slave sends an acknowledge bit to indicate that the register address has been received. The master then transfers the data 8 bits at a time, with the slave sending an acknowledge bit after each 8 bits. The PO2030N uses 8 bit data for its internal registers, thus requiring one 8-bit transfer to write to one register. After 8 bits are transferred, the register address is automatically incremented, so that the next 8 bits are written to the next register address. The master stops writing by sending a start or stop bit.

A typical read sequence is executed as follows. First the master sends the write-mode slave address and 8-bit register address just as in the write request. The master then sends a start bit and the read-mode slave address. The master then clocks out the register data 8 bits at a time. The master sends an acknowledge bit after each 8-bit transfer. The register address is auto-incremented after each 8 bit is transferred. The data transfer is stopped when the master sends a no-acknowledge bit.

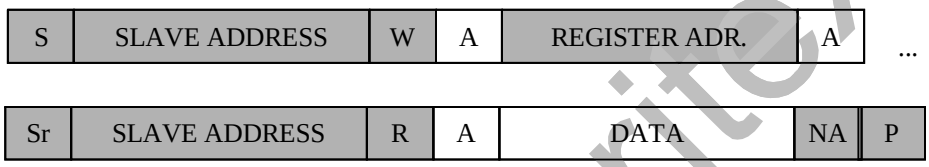
I²C Functional Description

Single Write Mode operation

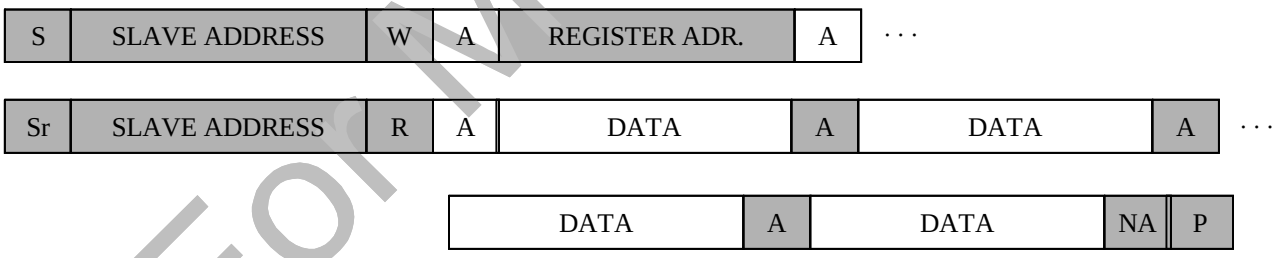
Multiple Write Mode (Register address is increased automatically)[1] operation



Single Read Mode operation



Multiple Read Mode (Register address is increased automatically)[1] operation



S: Start condition. Sr : Repeated Start (Start without preceding stop.)
SLAVE ADDRESS: write address = DCh = 11011100b
read address = DDh = 11011101b
R/W: Read/Write selection. High = read / LOW = write.
A: Acknowledge bit. NA : No Acknowledge.
DATA: 8-bit data
P: Stop condition

Note 1: Continuous writing or reading without any interrupt increases the register address automatically. If the address is increased above valid register address range, further writing does not affect the chip operation in write mode. Data from invalid registers are undefined in read mode.

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Register Table

Address	Name	R/W	Default Value	Description
0(00h)	DeviceID_H	R	00100000	PO2030N Device ID
1(01h)	DeviceID_L	R	00110000	
2(02h)	RevNumber	R	00000011	PO2030N Revision number
4(04h)	FrameWidth_H	R/W	xx000011	Frame Width = 899d(0383h)
5(05h)	FrameWidth_L	R/W	10000011	
6(06h)	FrameHeight_H	R/W	xx000001	Frame Height = 499d(01F3h)
7(07h)	FrameHeight_L	R/W	11110011	
8(08h)	WindowX1_H	R/W	00000000	Window X1 = 208d (00D0h)
9(09h)	WindowX1_L	R/W	11010000	
10(0Ah)	WindowY1_H	R/W	00000000	Window Y1 = 8d (0008h)
11(0Bh)	WindowY1_L	R/W	00001000	
12(0Ch)	WindowX2_H	R/W	00000011	Window X2 = 848d (0350h)
13(0Dh)	WindowX2_L	R/W	01010000	
14(0Eh)	WindowY2_H	R/W	00000001	Window Y2 = 488d(01E8h)
15(0Fh)	WindowY2_L	R/W	11101000	
18(12h)	AmpBias	R/W	xxxx0010	Global Current Bias
19(13h)	PixelBias	R/W	xxxx0010	Pixel Array Current Bias
21(15h)	GlobalGain	R/W	00000000	Gain Factor that is Common to R, G, B
22(16h)	RedGain	R/W	01000000	R Pixel Gain Factor
23(17h)	Green1Gain	R/W	01000000	G1 Pixel Gain Factor
24(18h)	BlueGain	R/W	01000000	B Pixel Gain Factor
25(19h)	Green2Gain	R/W	01000000	G2 Pixel Gain Factor
26(1Ah)	ExpTime_H	R/W	xx000000	Integration Time Control
27(1Bh)	ExpTime_M	R/W	10000000	
28(1Ch)	ExpTime_L	R/W	000000xx	
29(1Dh)	Tgcontrol1	R/W	00000000	Timing Generate Control Registers
30(1Eh)	Tgcontrol2	R/W	00001010	
31(1Fh)	Tgcontrol3	R/W	00011001	
32(20h)	Tgcontrol4	R/W	01000100	
56(38h)	ADCOffset	R/W	00000000	ADC offset = 0d
70(46h)	FdControl	R/W	00000000	Flicker Control Register
75(4Bh)	regclk167	R/W	00101100	
76(4Ch)	Period50H	R/W	00010010	Flicker Period(50Hz) = (15 Frame) 75d X 64
77(4Dh)	Period50L	R/W	11000000	
78(4Eh)	Period60H	R/W	00001111	Flicker Period(60Hz) = (15 Frame) 62d X 64
79(4Fh)	Period60L	R/W	10000000	
80(50h)	IspControl1	R/W	11111101	ISP Control Registers
81(51h)	IspControl2	R/W	00000000	
82(52h)	IspControl3	R/W	01001010	
83(53h)	IspControl4	R/W	00101000	
84(54h)	IspControl5	R/W	11000000	
89(59h)	RGmmCoeff0	R/W	00000000	Red Gamma Coefficients
90(5Ah)	RGmmCoeff1	R/W	00000110	
91(5Bh)	RGmmCoeff2	R/W	00001011	
92(5Ch)	RGmmCoeff3	R/W	00011110	
93(5Dh)	RGmmCoeff4	R/W	00110001	
94(5Eh)	RGmmCoeff5	R/W	01001001	

Address	Name	R/W	Default Value	Description
95(5Fh)	GmmCoeff6	R/W	01100001	Common Gamma Coefficients
96(60h)	GmmCoeff7	R/W	10000100	
97(61h)	GmmCoeff8	R/W	10100010	
98(62h)	GmmCoeff9	R/W	10111101	
99(63h)	GmmCoeff10	R/W	11011000	
100(64h)	GmmCoeff11	R/W	11101100	
111(6Fh)	ColorMatrix11	R/W	00111000	Color Correction Coefficients
112(70h)	ColorMatrix12	R/W	10100101	
113(71h)	ColorMatrix13	R/W	00001101	
114(72h)	ColorMatrix21	R/W	10010011	
115(73h)	ColorMatrix22	R/W	00101101	
116(74h)	ColorMatrix23	R/W	00000110	
117(75h)	ColorMatrix31	R/W	10000011	
118(76h)	ColorMatrix32	R/W	10101010	
119(77h)	ColorMatrix33	R/W	01001101	
121(79h)	Edgegain	R/W	10101100	Edge Enhancement Factor E66:E106
123(7Bh)	EdgeTh	R/W	00000011	Edge Enhancement Threshold
126(7Eh)	CG11C	R/W	00100000	Cb Color Gain
127(7Fh)	CG22C	R/W	00100000	Cr Color Gain
128(80h)	Bright	R/W	00000000	Y Brightness = 16d(10h)
129(81h)	Contrast	R/W	10010100	Y Contrast. 80h = x1
131(83h)	BlankEAV	R/W	10110000	CCIR 656 synchronization purposes
132(84h)	ActiveEAV	R/W	10010000	
133(85h)	BlankSAV	R/W	10100000	
134(86h)	ActiveSAV	R/W	10000000	
135(87h)	VsyncStart_H	R/W	00000000	Out Vsync Row Start = 8d(0008h)
136(88h)	VsyncStart_L	R/W	00001000	
137(89h)	VsyncStop_H	R/W	00000001	Out Vsync Row Stop = 488d(01E8h)
138(8Ah)	VsyncStop_L	R/W	11101000	
139(8Bh)	VsyncColumn_H	R/W	00000000	Out Vsync Column Start = 1d(0001h)
140(8Ch)	VsyncColumn_L	R/W	00000001	
141(8Dh)	AutoControl	R/W	00000011	Auto(Exposure/White Balance) Control Register
142(8Eh)	BMinAwb	R/W	00000000	Minimum AWB B Gain
143(8Fh)	BMaxAwb	R/W	11111111	Maximum AWB B Gain
144(90h)	CbTone	R/W	10000000	Cb sepia Data
145(91h)	CrTone	R/W	10000000	Cr sepia Data
146(92h)	RefExp	R/W	00111000	Y Bright Target = 56d(38h)
147(93h)	MinGlbGain	R/W	00000000	Minimum Global Gain = 5d(05h)
148(94h)	MaxGlbGain	R/W	00100000	Maximum Global Gain = 5d(05h)
149(95h)	AeLock	R/W	00000110	Auto Exposure(AE) Lock range
153(99h)	MaxExpTime_H	R/W	00000001	Maximum Frame Height
154(9Ah)	MaxExpTime_L	R/W	11110011	
157(9Dh)	AwbRed	R/W	10000000	AWB Red Bias
158(9Eh)	AwbBlue	R/W	10000000	AWB Blue Bias
159(9Fh)	RMinAwb	R/W	00000000	Minimum AWB R Gain
160(A0h)	RMaxAwb	R/W	11111111	Maximum AWB R Gain
161(A1h)	weightx1_H	R/W	00000001	Weight Window : X1 = 421d(01A5h)
162(A2h)	weightx1_L	R/W	10100101	

Address	Name	R/W	Default Value	Description
163(A3h)	weightx2_H	R/W	00000010	Weight Window : X2 = 634d(027Ah)
164(A4h)	weightx2_L	R/W	01111010	
165(A5h)	weighty1_H	R/W	00000000	Weight Window : Y1 = 167d(00A7h)
166(A6h)	weighty1_L	R/W	10101000	
167(A7h)	weighty2_H	R/W	00000001	Weight Window : Y2 = 327d(0147h)
168(A8h)	weighty2_L	R/W	01001000	
200(C8h)	green_gm0	R/W	00000000	Green Gamma Coefficients.
201(C9h)	green_gm1	R/W	00000110	
202(CAh)	green_gm2	R/W	00001011	
203(CBh)	green_gm3	R/W	00011110	
204(CCh)	green_gm4	R/W	00110001	
205(CDh)	green_gm5	R/W	01001001	
206(CEh)	blue_gm0	R/W	00000000	Blue Gamma Coefficients.
207(CFh)	blue_gm1	R/W	00000110	
208(D0h)	blue_gm2	R/W	00001011	
209(D1h)	blue_gm3	R/W	00011110	
210(D2h)	blue_gm4	R/W	00110001	
211(D3h)	blue_gm5	R/W	01001001	
212(D4h)	CG12C	R/W	00000000	Cr Factor in Cb Data
213(D5h)	CG21C	R/W	00000000	Cb Factor in Cr Data
214(D6h)	LensG	R/W	xxxx0000	Lens Shading Gain

Register Descriptions

Register names are written in *slanted* characters. To differentiate between decimal, binary, and hexa numbers, (d, b, and h) are appended. The sensor should be reset by RSTB pin set low, after power is up, for at least 8 master clock periods. This will initialize all of the registers to their default values.

(0-2) *DeviceID, RevNumber*

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
00h	0	0	1	0	0	0	0	0	R
01h	0	0	1	1	0	0	0	0	
02h	X	X	X	X	0	0	1	1	

Device ID : 2030h => PO2030
Revision Number : 03h => N

(4-5) *FrameWidth*

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
04h	X	X	0	0	0	0	1	1	R/W
05h	1	0	0	0	0	0	1	1	

Maximum : 16,383d(3FFFh)
Default : 899d(0383h)
Description :

FrameWidth is the number of columns to be counted during one line time. Column counter value is incremented 1 by 1 until it reaches *FrameWidth*, then it is reset to 0. It can be larger than physical frame width but cannot be smaller. *FrameHeight* and *FrameWidth* determines the frame rate. Frame rate is given as

freq(Internal Pixel Clock) / *((FrameHeight* +1*)* X *(FrameWidth*+1 *))*

For example, freq(Internal Pixel Clock) = 4.5 MHz, *FrameHeight* = 499 and *FrameWidth* = 899. then, the frame rate is 30 fps. If you double the *FrameWidth*, you cut the frame rate by half. *FrameWidth* value must be set with respect to the full sampling mode. Changing to 1/4 or 1/16 sub-sampling mode does not require any change in *FrameWidth*.

(6-7) *FrameHeight*

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
06h	X	X	0	0	0	0	0	1	R/W
07h	1	1	1	1	0	0	1	1	

Maximum : 16,383d = 3FFFh

Default : 499d = 01F3h

Description :

FrameHeight is the number of rows to be counted during one frame time. Row counter value is incremented 1 by 1 until it reaches *FrameHeight*, then it is reset to 0. It can be larger than physical frame height but cannot be smaller. *FrameHeight* and *FrameWidth* determines the frame rate. Frame rate is given as

freq(Internal Pixel Clock) / *((FrameHeight* +1) X *((FrameWidth*+1 *))*

For example, freq(Internal Pixel Clock) = 4.5 MHz, *FrameHeight* = 499 and *FrameWidth* = 899. Then, the frame rate is 30 fps. If you double the *FrameHeight*, you cut the frame rate by half, and the vertical blank time is increased, but the PCLK rate does not change.

(8-9) *WindowX1*

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
08h	X	X	0	0	0	0	0	0	R/W
09h	1	1	0	1	0	0	0	0	

Default : *Window X1* = 208d (00D0h)

Description :

Window can be defined by 4 parameters : *WindowX1, WindowY1, WindowX2,* and *WindowY2.* Serial image data stream out pixel by pixel. Window specifies the area of pixels that we are interested in. HSYNC signal indicates if the image data output is from a pixel that lies within the window area or not.

Output data stream does not stop for pixels lying outside the window : just the HSYNC signal is de-asserted. The actual window position in the frame is given as

upper right corner = (*Window X1*, *Window Y1*)
lower left corner = (*Window X2*, *Window Y2*)

All the coordinates are with respect to the maximum window origin (0, 0) of Figure 3. Window position and size is with respect to the full sampling mode. It is not necessary to change the window parameters when sampling mode is switched between one and another.

(10-11) *WindowY1*

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
0Ah	X	X	0	0	0	0	0	0	R/W
0Bh	0	0	0	0	1	0	0	0	

Default : *Window Y1* = 8d (0008h)
Description : refer to *Window X1*.

(12-13) *WindowX2*

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
0Ch	X	X	0	0	0	0	1	1	R/W
0Dh	0	1	0	1	0	0	0	0	

Default : *Window X2* = 848d (0350h)
Description : refer to *Window X1*.

(14-15) *WindowY2*

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
0Eh	X	X	0	0	0	0	0	1	R/W
0Fh	1	1	1	0	1	0	0	0	

Default : *Window Y2* = 488d (01E8h)
Description : refer to *Window X1*.

(18) *Amp Bias*

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
12h	X	X	X	X	0	0	1	0	R/W

Description :

All analog circuits such as opamp or reference voltage generators are biased using current mirrors. Current flowing in every branch of analog circuits is an integral multiple of 1uA.

Ibranch = (*Global I Bias*) * 1uA

If an opamp has 4 branches and *Global I Bias* is set to 2, then the amplifier consumes total current of 8uA . As the current increases, frequency response of opamp improves and better images can be obtained, but the power consumption also increases.

(19) *Pixel Bias*

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
13h	X	X	X	X	0	0	1	0	R/W

Default : *PixelBias* = 2d (02h)

Description :

Pixel array has a source follower circuit for each column to buffer the photo-diode signal voltage. The source follower bias current is determined as an integral multiple of 1uA.

Ipixel = *PixelBias* * 1uA

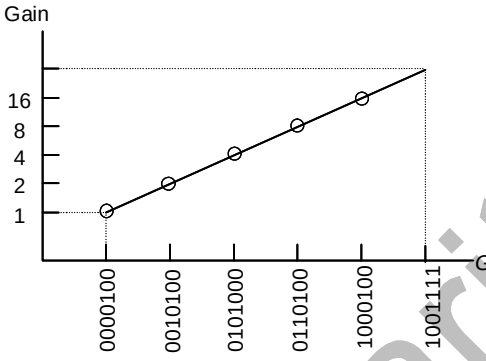
(21) *Global Gain*

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
15h	0	0	0	0	0	0	0	0	R/W

Default : *GlobalGain* = *0*d (00h)

Description :

GlobalGain has effect on all of R, G, and B pixel outputs. Raw R, G, B data are amplified by a common factor of *GlobalGain*. The relation between *GlobalGain* and amplification factor is shown in the picture below. Maximum value of *GlobalGain* is 1001111. Gain factors for *GlobalGain* larger than or equal to 1010000 are not defined.



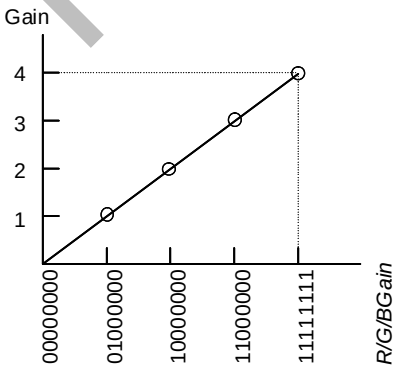
(22) *RGain*

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
16h	0	1	0	0	0	0	0	0	R/W

Default : *Rgain* = *64*d (40h)

Description :

RGain is the multiplication factor for red pixel output. Total gain factor for red pixels is (gain from *GlobalGain*) * (gain from *Rgain*).



R / G / B gain can be used for white balance control. Bit7 of *R/G/BGain* is weighted by 2, bit6 by1 and the other consecutive bits are weighted by 1/2, 1/4, 1/8, … respectively. That is, *R/G/Bgain* is a binary number with decimal point between bit6 and bit5.

(23) *G1Gain*

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
17h	0	1	0	0	0	0	0	0	R/W

Default : G1*gain* = *64*d (40h)

Description :

G1 pixels are those green pixels whose nearest neighbors are red pixels.

Refer to *RGain* register description.

(24) *BGain*

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
18h	0	1	0	0	0	0	0	0	R/W

Default : *Bgain* = *64*d (40h)

Description : refer to *RGain* register description.

(25) *G2Gain*

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
19h	0	1	0	0	0	0	0	0	R/W

Default : *G2gain* = *64*d (40h)

Description :

G2 pixels are those green pixels whose nearest neighbors are blue pixels.

Refer to *RGain* register description.

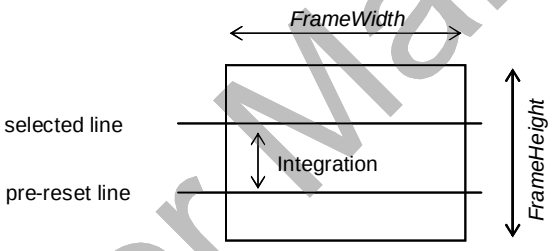
(26-28) *IntTime*

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
1Ah	X	X	0	0	0	0	0	0	R/W
1Bh	1	0	0	0	0	0	0	0	R/W
1Ch	0	0	0	0	0	0	X	X	R/W

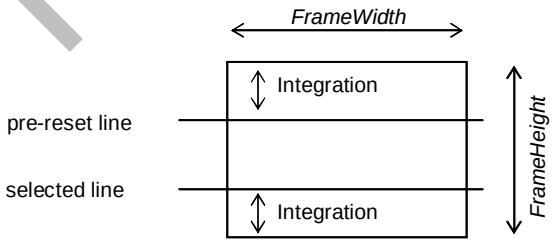
Description :

There are 3 bytes of registers to control the photo-charge accumulation interval for each pixel. 1Ah and 1Bh registers indicate how many line times the integration will continue until they are all reset. 1Ch register further sub-divides one line time into 64 smaller intervals. Total integration time is the sum of the integral multiple and fractional parts of one line time.

As the row counter value is incremented from 0 to *FrameHeight*, each line relevant to the row count is selected and all pixel data of that line is read out all at once. The read-out operation involves pixel reset pulses, so all pixels that are selected and read out are reset to initial states. To control exposure time, there runs another counter to select and reset a line other than the one that is selected to be read out. The space between the two lines is equal to the number of integration lines. There are two possible situations concerning the position of selected line and reset line. The 1st case is where the pre-reset counter runs ahead of read-out counter. And the other case Is just the reverse of the 1st one. The number of integration lines is different for the two cases as is shown in the left figures.



Case 1. Reset line preceding select line



Case 2. Select line preceding reset line

Since the basic unit of integration time for PO2030N is 1/ 64 line time, it is easy to implement Auto Exposure algorithms without worrying about strong light environment where the image may change abruptly in brightness or it may even blink.

(29) Timing Generator Control Register 1

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Read/Write
1Dh	Drop	CK2	CK1	CK0	X	X	X	X	R/W
	0	0	0	0	0	0	0	0	

Bit name	value	Description	
Drop	0 1	Frame Drop Disable. Frame Drop Enable.	
CK(2:0)	Mode / Value	YCbCr4:2:2, RGB565 RGB888	BayerRGB, Mono
	000	PCLK = MCLK(Default)	PCLK = MCLK x 1 / 2(Default)
	001	PCLK = MCLK x 2 / 3	PCLK = MCLK x 1 / 3
	010	PCLK = MCLK x 1 / 2	PCLK = MCLK x 1 / 4
	011	PCLK = MCLK x 1 / 4	PCLK = MCLK x 1 / 8
	100	PCLK = MCLK x 1 / 8	PCLK = MCLK x 1 / 16
	101	PCLK = MCLK x 1 / 16	PCLK = MCLK x 1 / 32
	110	PCLK = MCLK x 1 / 32	PCLK = MCLK x 1 / 64
	111	PCLK = MCLK x 1 / 64	PCLK = MCLK x 1 / 128

- When Sensor is under drop state, hsync and vsync drop.

(30) Timing Generator Control Register 2

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Read/Write
1Eh	HM	VM	ST	FT	X	X	X	X	R/W
	0	0	0	0	1	0	1	0	

Bit name	value	Description
HM	0 1	Horizontal Mirror Disable. Horizontal Mirror Enable.
VM	0 1	Vertical Mirror Disable. Vertical Mirror Enable.
ST	0 1	Electrical Shutter Selection Mechanical Shutter Selection
FT	0 1	Single Frame Transfer Disable. Single Frame Transfer Enable.

(31) Timing Generator Control Register 3

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Read/Write
1Fh	sync	stdby	BW	X	X	X	X	X	R/W
	0	0	0	1	1	0	0	1	

Bit name	value	Description
sync	0	Sync input register
stdby	0	Stdby input register
BW	0 1	Color Sensor Black & White Sensor

(32) Timing Generator Control Register 4

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Read/Write
20h	SM7	SM6	SM5	SM4	SM3	SM2	SM1	SM0	R/W
	0	1	0	0	0	1	0	0	

Default : *68d (44h)*

Description

MSB 4 bits control sub sampling mode under Video State, while LSB 4bits under Still State.

Under Video State,

sm(6) & sm(5) : "1X" => VGA
sm(6) & sm(5) : "00" => QVGA
sm(6) & sm(5) : "01" => QQVGA

Under Still State,

sm(2) & sm(1) : "1X" => VGA
sm(2) & sm(1) : "00" => QVGA
sm(2) & sm(1) : "01" => QQVGA

bit7 and bit3 must set '0' : This is used for Sensor Sub-sampling Enable S/W under Video/Still State each other. These bits not used for PO2030N.

bit4 and bit0 are reserved bits for PO2030N

(56) ADC offset

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
38h	0	0	0	0	0	0	0	0	R/W

Default : ADC offset = *0*d (00h)

Description :

ADC offset value.

(70) Flicker Control Register 1

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Read/Write
46h	AF	F5	F6	FDM	FK1	FK0	FL1	FL0	R/W
	0	0	0	0	0	0	0	0	

Default : *00d (00h)*

Bit name	value	Description
AF	0 1	Manual Flicker Detection Enable Mode. Auto Flicker Detection Enable Mode
F5	0 1	50Hz Flicker Detection Mode Disable 50Hz Flicker Detection Mode Enable
F6	0 1	60Hz Flicker Detection Mode Disable 60Hz Flicker Detection Mode Enable
FDM	0 1	Flicker Duration long lasting Mode Flicker Duration only while the flicker exists.
FK (1:0)	00 01 10 11	Flicker Count Increase/Decrease step ‘0’. Flicker Count Increase/Decrease step ‘1’. Flicker Count Increase/Decrease step ‘2’. Flicker Count Increase/Decrease step ‘3’.
FL(1:0)	00 01 10 11	Flicker Tolerance ‘0’ Flicker Tolerance ‘1’ Flicker Tolerance ‘2’ Flicker Tolerance ‘3’

(75) Regclk167

Address	Name	Function	Read/Write
4Bh	regclk167	# of Master clock divide by flicker detection standard time	R/W

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
4Bh	0	0	1	0	1	1	0	0

Regclk167 = 1.667ms * master clock freq. / 256

Description :
# of Master clock for flicker detection standard time or 1.667 ms time ratio

(76-79) Flicker Free Mode Registers

Address	Name	Function	Read/Write
4Ch	period50 (H)	Flicker Period Control register for 50Hz light source	R/W
4Dh	period50 (L)		
4Eh	period60 (H)	Flicker Period Control register for 60Hz light source	R/W
4Fh	period60 (L)		

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
4Ch	0	0	0	1	0	0	1	0
4Dh	1	1	0	0	0	0	0	0
4Eh	0	0	0	0	1	1	1	1
4Fh	1	0	0	0	0	0	0	0

Description :

Refer to the application note (page 62)

(80) ISP Control Register 1

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Read/Write
50h	X	X	X	CCE	X	X	SCE	X	R/W
	1	1	1	1	1	1	0	1	

Description :

mnemonic	Description	ON	OFF
CCE	Color Correction Enable	1	0
SCE	Sepia Color Enable	1	0

(1) CCE : *Related Registers* : reg. 6Fh ~ 77h(Color Correction Coefficients)

'1' : (default) Color Correct Enable

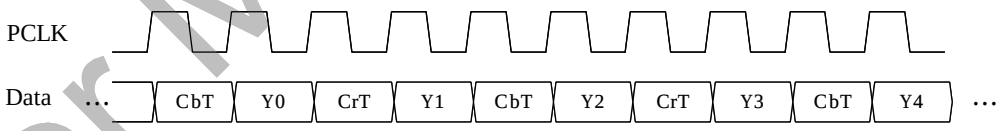
'0' : Bypass. Color Correct Disable.

(2) SCE : *Related Registers* : reg. 90h(Cb Tone) ~ 91h(Cr Tone)

'1' : Output Cb/Cr keep on Cb/Cr_Tone Data.

'0' : (default) Normal condition.

* SCE is only effected on that output data form is related Y,Cb,Cr.



(81) ISP Control Register 2

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Read/Write
51h	CEN	CCT2	CCT1	CCT0	ODF3	ODF2	ODF1	ODF0	R/W
	0	0	0	0	0	0	0	0	

Description :

mnemonic	Description
CEN	Out Clock OFF('1') / On('0')
CCT[2:0]	Out Clock Control
ODF[3:0]	Out Data Format

(1) CEN

'1' : output clock set to ground.

'0' : normal condition.

(2) CCT[2:0] : Out Clock format Control.

"000" : normal "001" : invert

"010" : & H-ref "011" : invert & H-ref

"100" : & V-ref "101" : invert & V-ref

"110" : & H-ref & Vref

(3) ODF[3:0] : Out Data Format

"0000" : CB Y CR Y "0001" : CR Y CB Y

"0010" : Y CB Y CR "0011" : Y CR Y CB

"0100" : RGRG...GBGB "0101" : GBGB...RGRG

"0110" : GRGR...BGBG "0111" : BGBG…GRGR

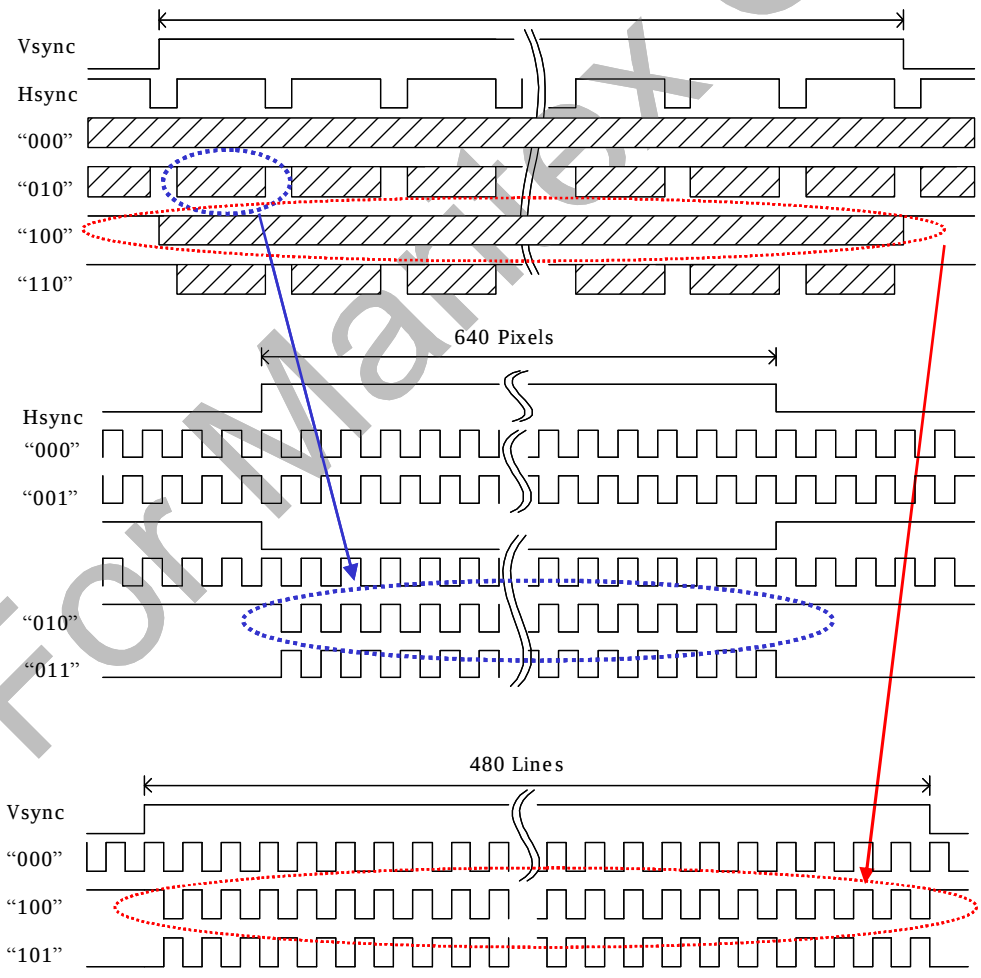
"1000" : R5G3, G3B5 "1001" : B5G3, G3R5

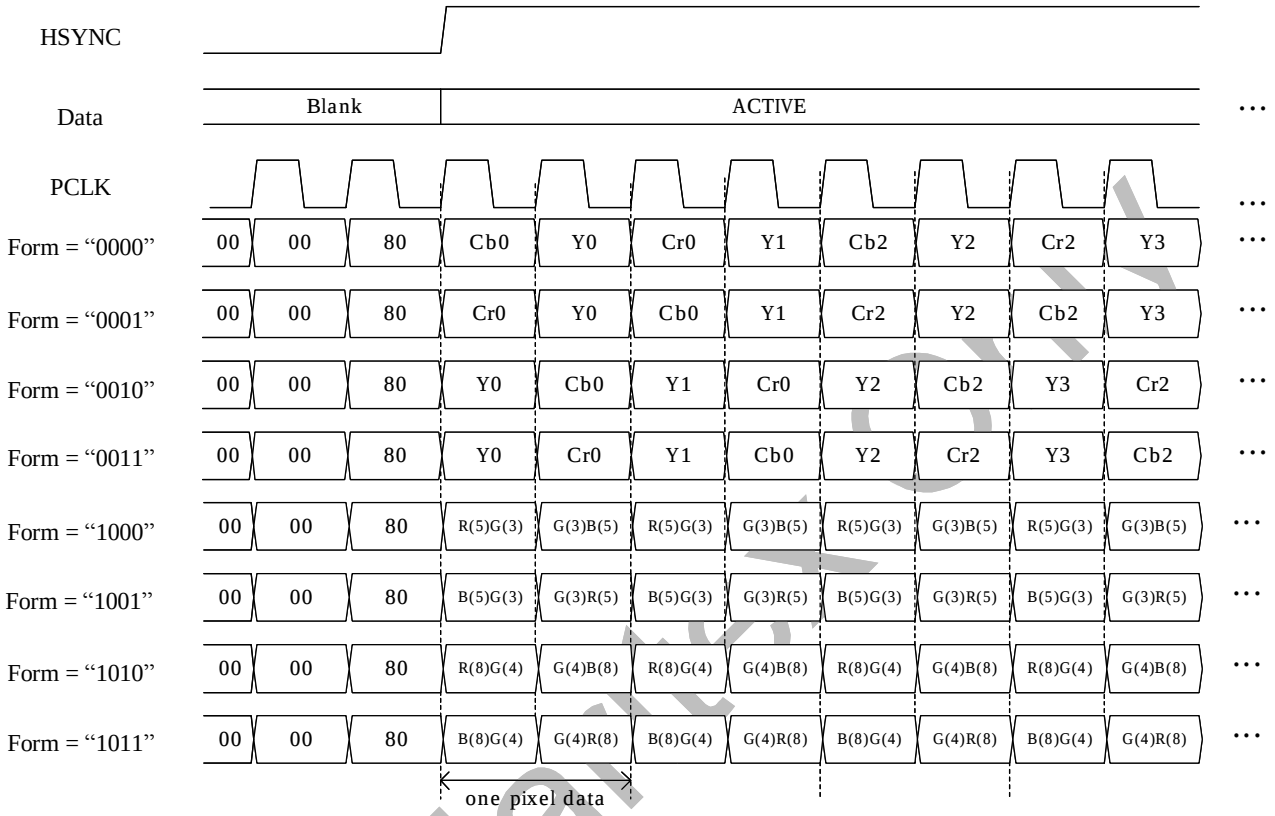
"1010" : R8G4,G4B8 "1011" : B8G4,G4B8

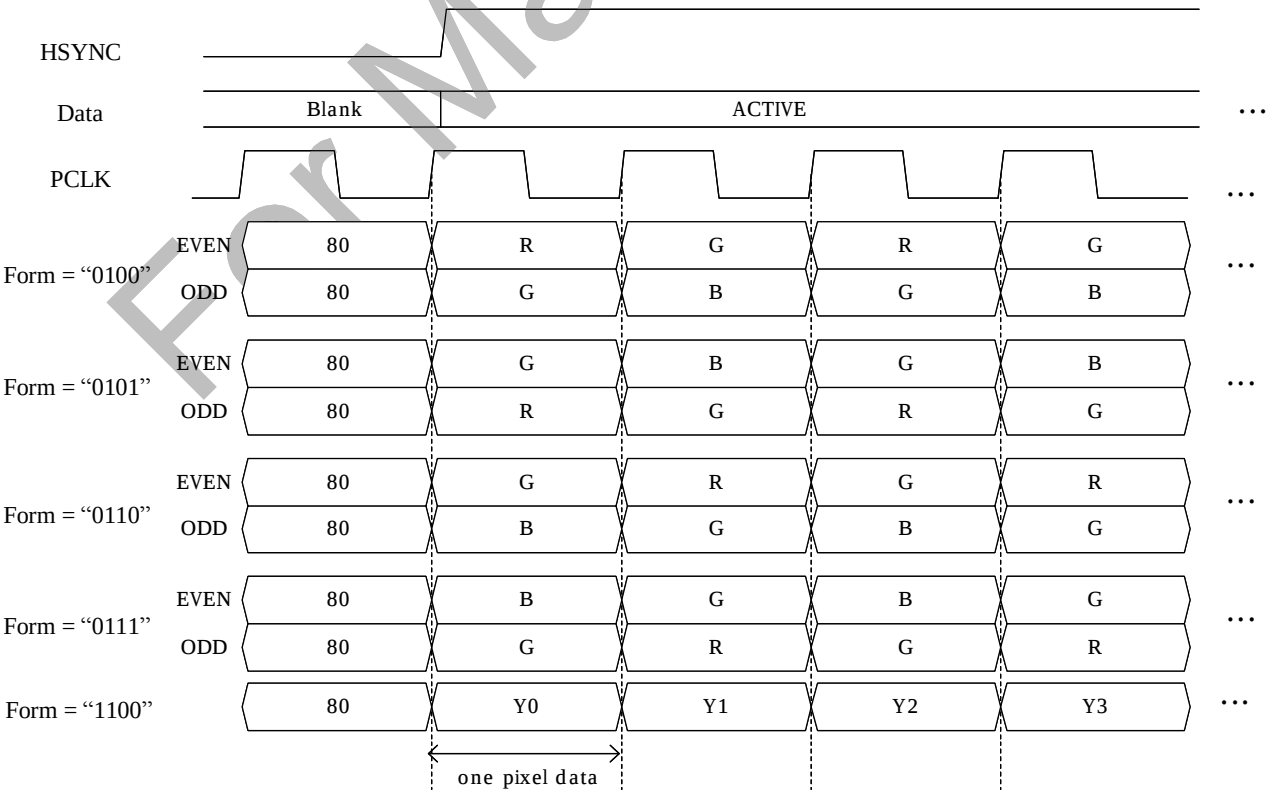
"1100" : YYYY...

- CCT[2:0] : Out Clock format

PCLK		Description
Normal type	Complementary type	
000	001	Normal Clock.(default)
010	011	Valid in Hsync high.
100	101	Valid in Active Window.
110	-	Valid in Active Window and Hsync high.







(82) ISP Control Register 3

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Read/Write
52h	Hi-z	SVS	Vpol	Hpol	HD	x	x	x	R/W
	0	1	0	0	1	0	1	0	

Description :

mnemonic	Description
Hi-z	Hi-Z. Output Pad Hi-Z, Default = '0'
SVS	VSYNC(1) ? V_reference(0)
Vpol	VSYNC(0) ? (not VSYNC(1))
Hpol	HSYNC(0) ? (not HSYNC(1))
HD	Active Region(0) ? All region(1) HSYNC

(1) Hi-z : '1' - Out Pad set to Hi-z conditions. '0' – Normal

(2) SVS :

'1' – variable type of Vsync

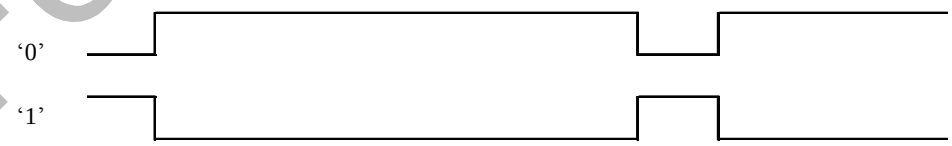
(Control by VSYNC Start(87h, 88h), VSYNC Stop(89h, 8Ah), VsyncColumn(8Bh, 8Ch))

'0' – constant type vsync

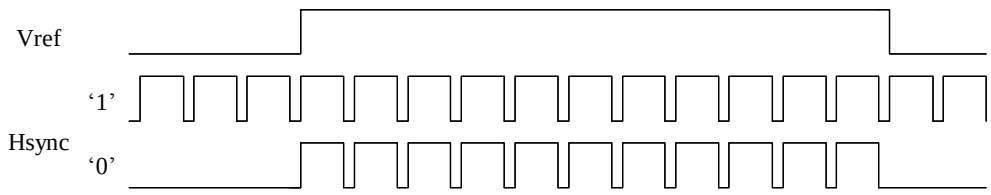
(Vsync Start = Y1(Reg.0Ah, 0Bh), VsyncStop = Y2(0Eh, 0Fh), VsyncColumn = 1)

(3) Vpol : VSYNC Invert.

(4) Hpol : HSYNC Invert.



(5) HD



(83) ISP Control Register 4

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Read/Write
53h	X	X	FY	X	X	RGE	GGE	BGE	R/W
	0	0	1	0	1	0	0	0	

Description :

mnemonic	Description
FY	Free Y. Y Data Clamped by '1'(1 ~ 254) or '0': (16 ~ 235)
RGE	R Gamma ON(0) / OFF(1)
GGE	G Gamma ON(0) / OFF(1)
BGE	B Gamma ON(0) / OFF(1)

(1) FY : '0' : $16 \le Y \le 235$ '1' : $1 \le Y \le 254$

(2) RGE, GGE, BGE : Red/Green/Blue Gamma '0'(ON), '1'(OFF)

(84) ISP Control Register 5

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Read/Write
54h	HDC	VDC	X	X	X	X	X	X	R/W
	1	1	0	0	0	0	0	0	

Description :

mnemonic	Description
HDC	Hsync Drop Condition Enable(1) / Disable(0).
VDC	Vsync Drop Condition Enable(1) / Disable(0).

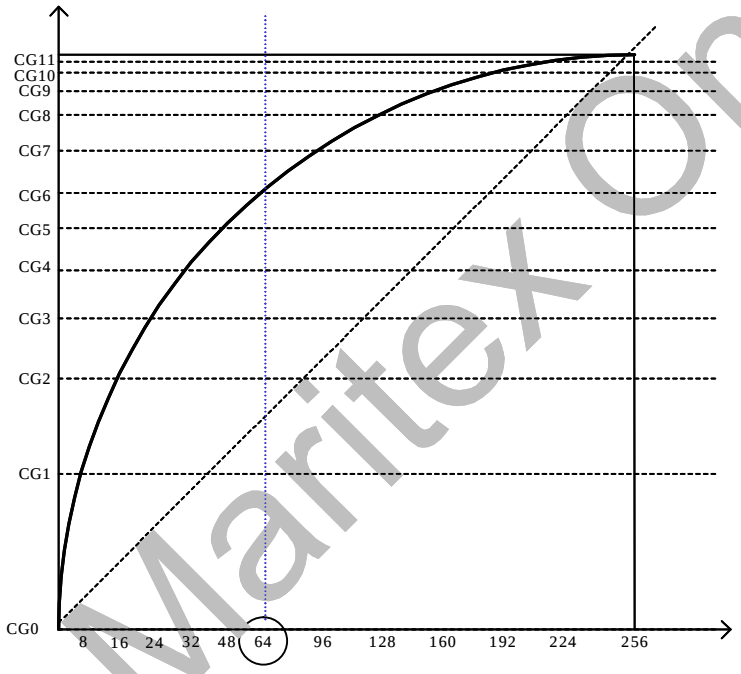
- HDC, VDC : '1' : enable drop conditions(register setting, drop state @ Still state)
'0' : disable drop conditions.

(89 ~ 100) ,
(200 ~ 211) Gamma Correction

Address	Name		Value	Read/Write
59h	*R*	*GC0*	0 0 0 0 0 0 0 0 (00h)	R/W
5Ah		*GC1*	0 0 0 0 0 1 1 0 (06h)	
5Bh		*GC2*	0 0 0 0 1 0 1 1 (0Bh)	
5Ch		*GC3*	0 0 0 1 1 1 1 0 (1Eh)	
5Dh		*GC4*	0 0 1 1 0 0 0 1 (31h)	
5Eh		*GC5*	0 1 0 0 1 0 0 1 (49h)	
C8h	*G*	*GC0*	0 0 0 0 0 0 0 0 (00h)	
C9h		*GC1*	0 0 0 0 0 1 1 0 (06h)	
CAh		*GC2*	0 0 0 0 1 0 1 1 (0Bh)	
CBh		*GC3*	0 0 0 1 1 1 1 0 (1Eh)	
CCh		*GC4*	0 0 1 1 0 0 0 1 (31h)	
CDh		*GC5*	0 1 0 0 1 0 0 1 (49h)	
CEh	*B*	*GC0*	0 0 0 0 0 0 0 0 (00h)	
CFh		*GC1*	0 0 0 0 0 1 1 0 (06h)	
D0h		*GC2*	0 0 0 0 1 0 1 1 (0Bh)	
D1h		*GC3*	0 0 0 1 1 1 1 0 (1Eh)	
D2h		*GC4*	0 0 1 1 0 0 0 1 (31h)	
D3h		*GC5*	0 1 0 0 1 0 0 1 (49h)	
5Fh	*RGB*	*GC6*	0 1 1 0 0 0 0 1 (61h)	
60h		*GC7*	1 0 0 0 0 1 0 0 (84h)	
61h		*GC8*	1 0 1 0 0 0 1 0 (A2h)	
62h		*GC9*	1 0 1 1 1 1 0 1 (BDh)	
63h		*GC10*	1 1 0 1 1 0 0 0 (D8h)	
64h		*GC11*	1 1 1 0 1 1 0 0 (ECh)	

Description :

Gamma Correction is applied to RGBsignal which ranges from 0 to 255 to compensate non-linear characteristics of display brightness vs input brightness. In many cases, power function of 0.45 is used as gamma function for CRT display.



(111 ~ 119) Color Transform From RGB space to YCbCr Space and Color Correction

Address	Name	Function	Read/Write
6Fh	*CT0*	Color Correction Matrix Coefficient, ***m00***	R/W
70h	*CT1*	Color Correction Matrix Coefficient, ***m01***	
71h	*CT2*	Color Correction Matrix Coefficient, ***m02***	
72h	*CT3*	Color Correction Matrix Coefficient, ***m10***	
73h	*CT4*	Color Correction Matrix Coefficient, ***m11***	
74h	*CT5*	Color Correction Matrix Coefficient, ***m12***	
75h	*CT6*	Color Correction Matrix Coefficient, ***m20***	
76h	*CT7*	Color Correction Matrix Coefficient, ***m21***	
77h	*CT8*	Color Correction Matrix Coefficient, ***m22***	

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	
6Fh	0	0	1	1	1	0	0	0	(38h)
70h	1	0	1	0	0	1	0	1	(A5h)
71h	0	0	0	0	1	1	0	1	(0Dh)
72h	1	0	0	1	0	0	1	1	(93h)
73h	0	0	1	0	1	1	0	1	(2Dh)
74h	0	0	0	0	0	1	1	0	(06h)
75h	1	0	0	0	0	0	1	1	(83h)
76h	1	0	1	0	1	0	1	0	(AAh)
77h	0	1	0	0	1	1	0	1	(4Dh)

- Color Coefficient : sign[7] | integer [6:5] | fractional [4:0]

CC Coefficient

$$\begin{pmatrix} 1.739627 & -1.14441 & 0.404786 \\ -0.60387 & 1.413677 & 0.190193 \\ -0.10247 & -1.30942 & 2.411888 \end{pmatrix} \times 32 = \begin{pmatrix} 55.66805 & -36.6212 & 12.95316 \\ -19.3239 & 45.23768 & 6.08619 \\ -3.27892 & -41.9015 & 77.18042 \end{pmatrix} = \begin{pmatrix} 38 & A5 & 0D \\ 93 & 2D & 06 \\ 83 & AA & 4D \end{pmatrix}$$

(121) EdgeGain

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Read/Write
79h	X	X	X	EG4	EG3	EG2	EG1	EG0	R/W
	1	0	1	0	1	1	0	0	

Default : edge gain=*172*d (ACh)

Description :

- EdgeGain [4:0] : Edge Gain. 04h = x1

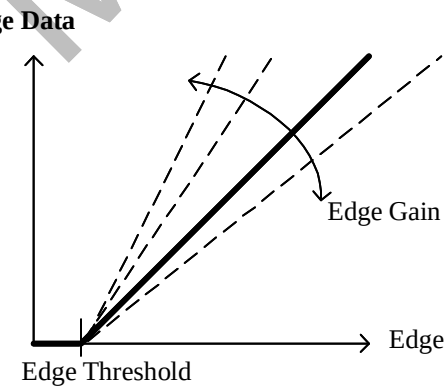
(123) Edge Threshold

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Read/Write
7Bh	0	0	0	0	0	0	1	1	R/W

Default : edge threshold =3d (03h)

Description :

Edge Enhancement threshold.



(126 ~ 127), (212 ~ 213) Color Gain & Color Rotation

Address	Name	Value	Read/Write
7Eh	CG11C	0 0 1 0 0 0 0 0 (20h)	R/W
7Fh	CG22C	0 0 1 0 0 0 0 0 (20h)	

Address	Name	Value	Read/Write
D4h	CG12C	0 0 0 0 0 0 0 0 (00h)	R/W
D5h	CG21C	0 0 0 0 0 0 0 0 (00h)	

Default : Color Gain 11 coefficient =32d (20h)
Color Gain 12 coefficient =0d (00h)
Color Gain 21 coefficient =0d (00h)
Color Gain 22 coefficient =32d (20h)

Description :

Color Gain & Color rotation matrix (cosine(θ), -sine(θ) ; sine (θ), cosine (θ))

- Sing[7] | Integer[6:5] | fractional[4:0]

$$\begin{bmatrix} CB' \\ CR' \end{bmatrix} = \begin{bmatrix} r11 & r12 \\ r21 & r22 \end{bmatrix} * \begin{bmatrix} cbgain & 0 \\ 0 & crgain \end{bmatrix} = \begin{bmatrix} r11*cbgain & r12*crgain \\ r21*cbgain & r22*crgain \end{bmatrix}$$

(128 ~ 129) Y Brightness and Contrast

Address	Name	Value	Read/Write
80h	Brightness	0 0 0 0 0 0 0 0 (00h)	R/W
81h	Contrast	1 0 0 1 0 1 0 0 (94h)	

Default : Brightness = 0d(00h)
Contrast = 148d(94h)

Description :

Y' = Y x (Y_contrast/128) + Y_bright

- brightness : sign[7] | integer[6:0]
- contrast : sign[7] | fractional[6:0]

(130) Cb/Cr Offset

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Read/Write
82h	1	0	0	0	0	0	0	0	R/W

Default : Cb / Cr Offset =*128*d (80h)

Description :

Cb/Cr range : -112 ~ +112

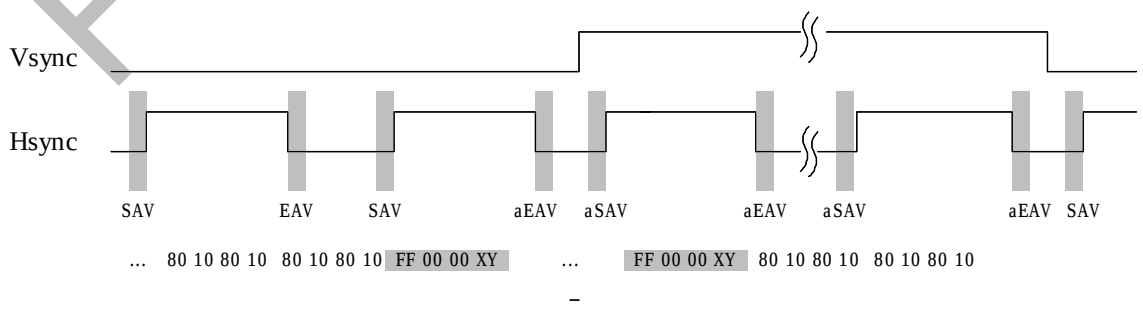
Cb / Cr data range : (-112 + CbCr_Offset) ~ (+112 + CbCr_Offset)

(131 ~ 134) CCIR656 Index Value

Address	Name	Description	Read/Write
83h	*BlankEAV*	Blank Range End of Video	R/W
84h	*ActiveEAV*	Active Range End of Video	
85h	*BlankSAV*	Blank Range Start of Video	
86h	*ActiveSAV*	Active Range Start of Video	

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	
83h	1	0	1	1	0	0	0	0	(B0h)
84h	1	0	0	1	0	0	0	0	(90h)
85h	1	0	1	0	0	0	0	0	(A0h)
86h	1	0	0	0	0	0	0	0	(80h)

Description : EAV and SAV signals are inserted for synchronization purposes.

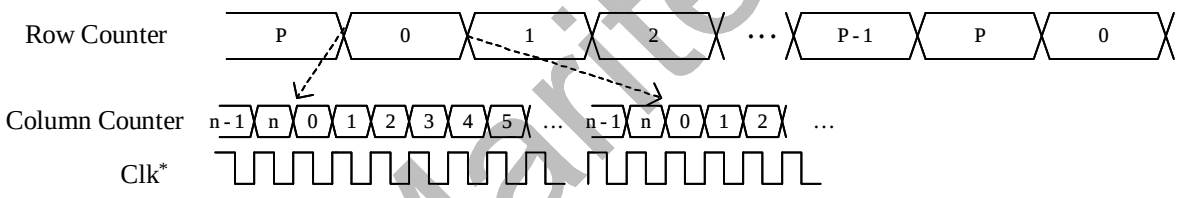


(135 ~ 140) Pad Vsync Start/ Stop

Address	Name	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	
87h	*VsyncStart (H)*	0	0	0	0	0	0	0	0	(00h)
88h	*VsyncStart (L)*	0	0	0	0	1	0	0	0	(08h)
89h	*VsyncStop (H)*	0	0	0	0	0	0	0	1	(01h)
8Ah	*VsyncStop (L)*	1	1	1	0	1	0	0	0	(E8h)
8Bh	*VsyncColumn (H)*	0	0	0	0	0	0	0	0	(00h)
8Ch	*VsyncColumn (L)*	0	0	0	0	0	0	0	1	(01h)

Description : VSYNC positions.

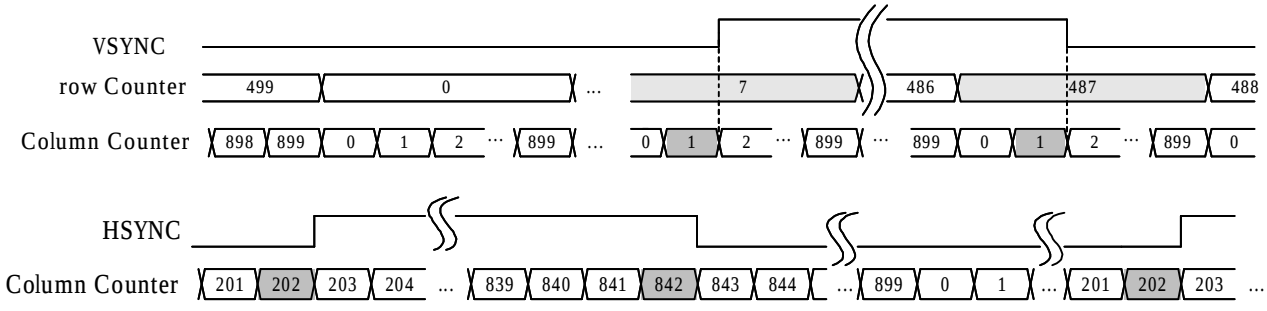
There are two counters to indicate the present coordinate of frame scanning :
Frame row counter and frame column counter. Counter values repeat the cycle of 0 to *Frame Height* , and 0 to *Frame Width* respectively.



P = reg. Frame Height
n = reg. Frame Width
CLK* : Clock for Bayer Data

VSYNC rising : when (Row_counter = Reg. VsyncStart) & (Column_counter = Reg. VsyncColumn)
falling : when (Row_counter = Reg. VsyncStop) & (Column_counter = Reg. VsyncColumn)

(For example) VsyncStart = 7d, VsyncStop = 487d, VsyncColumn = 0d.
Frame Width(reg.04h, 05h) = 899d, Frame Height(reg.06h, 07h) = 499d,
Window X1(reg. 08h, 09h) = 202d, Window X2(reg.0Ch, 0Dh) = 842d.
Then VSYNC & HSYNC is



(141) Auto Control 1

Address	Name	Function	Read/Write
8Dh	*AutoControl1*	Auto ISP Function Control I	R/W

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
X	X	X	WW1	WW0	FC	AWB	AE
0	0	X	0	0	0	1	1

mnemonic	Description
AE	**AE_EN (Auto Exposure Enable)** **Default** : '1' **Related Registers** : *RefExpTime[92h], MaxExpTime[97h:96h], ExpTime[1Ah-1Ch], AWBAELock[95h], Global Gain[15h], MinGlbGain[93h], MaxGlbGain[94h] :* '1' : auto exposure mode '0' : auto exposure mode off During the auto exposure mode, *Integration Lines, GlobalGain* registers cannot be written.
AWB	**AWB_EN (Auto White Balance Enable)** **Default** : '1' **Related Registers** : *AWBAELock[95h], AWBRed[9Dh], AWBBlue[9Eh]* '1' : auto white balance mode enabled '0' : auto white balance mode disenabled
FC	**FC (Flicker Canceling Enable)** **Default** : '0' **Related Registers** : *FdControl[46h], Period50[4Dh:4Ch], Period60[4Fh:4Eh], FdPeriod[ABh:Aah]* ISP is kept in flicker canceling mode according to *FdControl* register.

WW[1:0]	**WW[1:0] (Weighting window mode)** **Default** = "00" **Related Registers** : weighting window register [4Fh-56h] Brightness data within the weighting window [4Fh-56h] have weighting factor a ccording to the weighting window mode as follows; 00 : x1 01 : x2 10 : x4 11 : x8 As weighting factor is growing, central image brightness within the weighting w indow has more impact on overall auto exposure function. Size and mode of wei ghting window have also some effects on the resultant brightness of image after AE process.
[5]	**UNUSED** **Default** = 'X'

(142 ~ 143),
(159 ~ 160) Red /Blue Gain Min / Max

Address	Name	Description	Read/Write
8Eh	*BminAWB*	Minimum Blue Gain in AWB	R/W
8Fh	*BmaxAWB*	Maximum Blue Gain in AWB	
9Fh	*RminAWB*	Minimum Red Gain in AWB	
A0h	*RmaxAWB*	Maximum Red Gain in AWB	

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	
8Eh	0	0	0	0	0	0	0	0	(00h)
8Fh	1	1	1	1	1	1	1	1	(FFh)
9Fh	0	0	0	0	0	0	0	0	(00h)
A0h	1	1	1	1	1	1	1	1	(FFh)

Default : BlueMinAWB = 0d(00h), BlueMaxAWB = 255d(FFh)
RedMinAWB = 0d(00h), RedMaxAWB = 255d(FFh)

Related Register : Auto Control1[8Dh]

Description :

During AWB, *RedGain* and *BlueGain* varies to get well balanced image according to *AWB Tuning* registers. In those case, variation of Red,BlueGain's are bounded by *Min/Max Red/Blue Gain.*

(144 ~ 145) Cb Tone / Cr Tone

Address	Name	Value	Read/Write
90h	Cb Tone	1 0 0 0 0 0 0 0 (80h)	R/W
91h	Cr Tone	1 0 0 0 0 0 0 0 (80h)	

Default : Cb Tone= 128d(80h), Cr Tone = 128d(80h)

Related register : ISP Control1[50h]

Description :

Cb/Cr Color Tone @ sepia color condition.

(146) RefExpTime

Address	Name	Function	Read/Write
92h	*RefExpTime*	Reference exposure time in auto-exposure mode	R/W

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
92h	0	1	0	0	0	0	0	0

Related Registers : AutoControl[8Dh], MaxExpTime[99h:9Ah], ExpTime[1Ah-1Ch], AWBAELock[95h], Global Gain[15h], MinGlbGain[93h], MaxGlbGain[94h]

Description : (*about auto exposure*)

If *AE_EN* of *Auto Control1*[8Dh] register is set to '1', *RefExpTime*, *GlbGain* registers are automatically controlled by ISP to control overall brightness of sensor image. During auto exposure process, the brightness level of image is set by *RefExpTime* register. The average brightness of image is controlled to get close to *RefExpTime* register value with the margin set by *AWBAELock[3:0]* register. *ExpTime* register is controlled, at first. If integration line register are limited, global gain register is controlled. Variation of *GlbGain or ExpTime* register are limited by *MinGlbGain*, *MaxGlbGain* and *MaxExpTime* registers, respectively.

(147-148) Global Gain Limit in automatic exposure process

Address	Name	Function	Read/Write
93h	*MinGlbGain*	Minimum limit of global gain	R/W
94h	*MaxGlbGain*	Maximum limit of global gain	R/W

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
41h	0	0	0	0	0	0	1	1
42h	0	0	0	0	0	0	1	1

Max : Reg42h ≤ 4Fh

Related Registers : *Auto Control1*[3Eh], *Global Gain*[15h]

Description :

The lower and upper boundary of *Global Gain* register is determined by *Global Gain Min* , *Global Gain Max* register, respectively. If auto exposure mode is set on, global gain register is automatically controlled by ISP function. If auto exposure mode is set off, global gain register is manually controllable. For related description, refer to that of *Y_target Register*.

(149) AWBAE Lock

Address	Name	Function	Read/Write
95h	*AwbAeLock*	Set margin of Awb and AE functions	R/W

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
95h	0	0	0	0	0	1	1	0

Related Registers : *Auto Control*[8Dh]

Description :

AwbMargin := AwbAeLock[7:4]

AeMargin := AwbAeLock[3:0]

(153-154) MaxExpTime

Address	Name	Function	Read/Write
99h	*MaxExpTime (H)*	Maximum Exposure Time	R/W
9Ah	*MaxExpTime (L)*		

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
47h	0	0	0	0	0	1	0	0
48h	0	0	0	1	0	0	1	1

Related Register : *Auto Control1*[8Dh]

Description :

During auto exposure mode, maximum exposure time is set by *MaxExpTime* register. If user set the *MaxExpTime* register larger value so that *ExpTime* register have larger value than default(0413h), frame rate is automatically varied.

(157-158) AWB Tune

Address	Name	Function	Read/Write
9Dh	*AWBT-Red*	AWB Red Tuning	R/W
9Eh	*AWBT-Blue*	AWB Blue Tuning	R/W

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
9Dh	1	0	0	0	0	0	0	0
9Eh	1	0	0	0	0	0	0	0

Related Register : *Auto Control1*[8Dh]

Description :

Average R, G, B ratio of a sensor image could be controlled. The ratio between R to G, B to G can be controlled by *AWBTune* registers under the following equation,

$$\overline{B} = \frac{AWB_{BLUE}}{128} \times \overline{G} \qquad \overline{R} = \frac{AWB_{RED}}{128} \times \overline{G}$$

(161-168) Weighting Window

Address	Name	Function	Read/Write
A1h	*WeightX1 (H)*	X1 coordination of weight window of auto-exposure process	R/W
A2h	*WeightX1 (L)*		
A3h	*WeightX2 (H)*	X2 coordination of weight window of auto-exposure process	R/W
A4h	*WeightX2 (L)*		
A5h	*WeightY1 (H)*	Y1 coordination of weight window of auto-exposure process	R/W
A6h	*WeightY1 (L)*		
A7h	*WeightY2 (H)*	Y2 coordination of weight window of auto-exposure process	R/W
A8h	*WeightY2 (L)*		

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
A1h	0	0	0	0	0	0	0	1
A2h	1	0	1	0	0	1	0	1
A3h	0	0	0	0	0	0	1	0
A4h	0	1	1	1	1	0	1	0
A5h	0	0	0	0	0	0	0	0
A6h	1	0	1	0	0	1	1	1
A7h	0	0	0	0	0	0	0	1
A8h	0	1	0	0	0	1	1	1

Default : *WeightX1* = 0x01A5h, *WeightX2*= 0x027Ah, *WeightY1* = 0x00A7h, *WeightY2* = 0x0327h

WeighteX1 > 421d, *WeightedX2* < 634d
WeighteY1 > 167d, *WeightedY2* < 327d

Related Register : *Auto Control1*[8Dh]

Description :

Refer to the description of WW bit of *Auto Control1*[8Dh].

(200 ~ 211) Gamma Correction

Refer to Reg.59h ~ 64h description.

(212 ~ 213) Color Gain & Color Rotation

Refer to Reg.7Eh ~ 7Fh description.

(214) Lens Shading Gain

Address	Name	Value	Read/Write
D6h	*LensG*	X X X X 0 0 0 0 (00h)	RW

Description : Lens Shading Gain.

Electrical Characteristics

Absolute Maximum Ratings *

VDD Supply Voltage ---------- -0.3V to 3.5V
DC Voltage at any input pin ---------- -0.3V to VDD+0.3V
DC current at any input pin ---------- -10mA to +10mA
Storage Temperature ---------- -40°C to +125 °C

Table 4. DC Characteristics

Symbol	Descriptions	Min	Typ	Max	Unit
V_{DD}	Digital, Analog, Pixel VDD voltage relative to GND(DGND, AGND, PGND) level.	2.2	2.5	2.8	V
	Recommended VDD	2.4	2.5	2.6	V
HV_{DD}	High VDD(HVDD) voltage relative to GND(DGND) level.	2.2	2.5 or 2.8	3.1	V
I_{DD1}	Supply current at 15 fps. Currents are programmable through I2C serial interface.		25	32	mA
I_{DD2}	Standby supply current		4	12	uA
V_{IL1}	Input voltage LOW level			0.2VDD	V
V_{IH1}	Input voltage HIGH level	0.8VDD			V
V_{IL2}	Input voltage LOW level for SCL, SDA.			0.7	V
V_{IH2}	Input voltage HIGH level for SCL, SDA.	1.5			V
C_{IN}	Input pin capacitance			10	pF
V_{OL1}	Output Voltage LOW			0.1VDD	V
V_{OH1}	Output Voltage HIGH	0.9VDD			V
V_{OL2}	Output Voltage LOW level for SCL, SDA.			0.2	V
V_{OH2}	Output Voltage HIGH level for SCL, SDA.	VDD-0.2			V
I_{IN}	Input leakage current		0.005	1	uA

* Excessive stresses may cause permanent damage to the device.

Table 5. AC Characteristics (HVDD = 2.8V, Default register setting, 15pF Load)

Symbol	Descriptions	Min	Typ	Max	Unit
f_{MCLK}	Master clock Frequency			27	MHz
duty	Master clock duty cycle		50		%
t1	Master clock rise/fall time		10		ns
t2	PCLK rise/fall time		15		ns
t3	MCLK falling edge to HSYNC			15	ns
t4	MCLK falling edge to digital output			15	ns
t5	MCLK falling edge to PCLK rising edge			15	ns

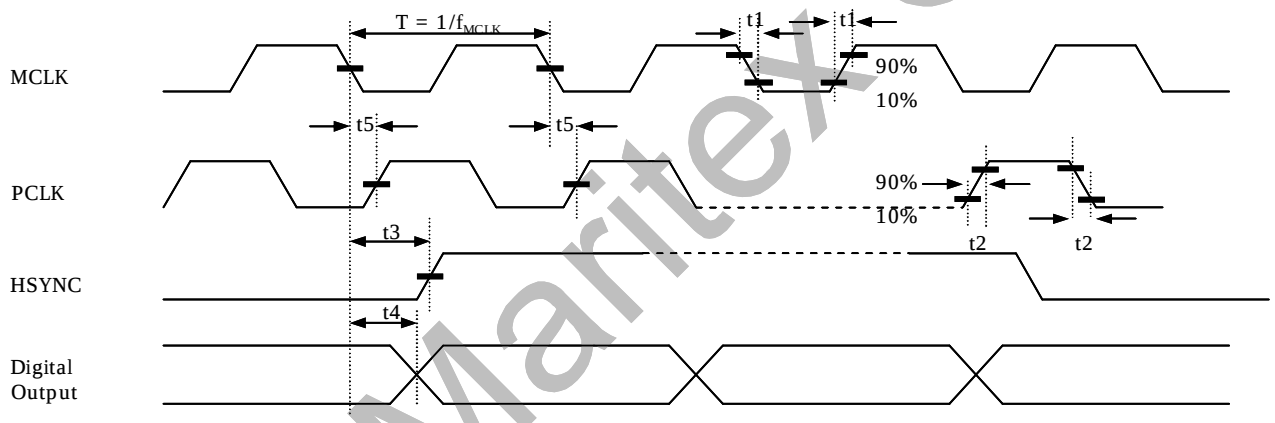


Fig. 13 Clock, Data, and Sync Timing.

Symbol	Descriptions	Min	Typ	Max	Unit
t6	Reset time	8			T

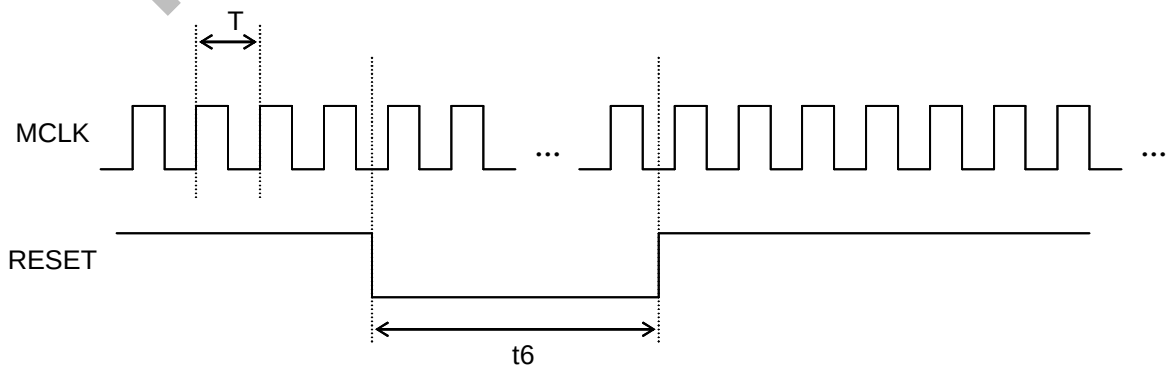


Table 12. Electro- Optical Characteristics

Symbol	Parameter	Notes	Min	Typ	Max	Unit
Sens	Sensitivity	1)		5.1		V/Lux.sec
Vsat	Saturation Level	2)		0.77	0.8	V
Vdrk	Dark Signal	3)		0.302		mV
PSNU	PIXEL Signal NON-Uniformity	4)		4	10	%
DR	Dynamic range	5)		68		dB

Notes :

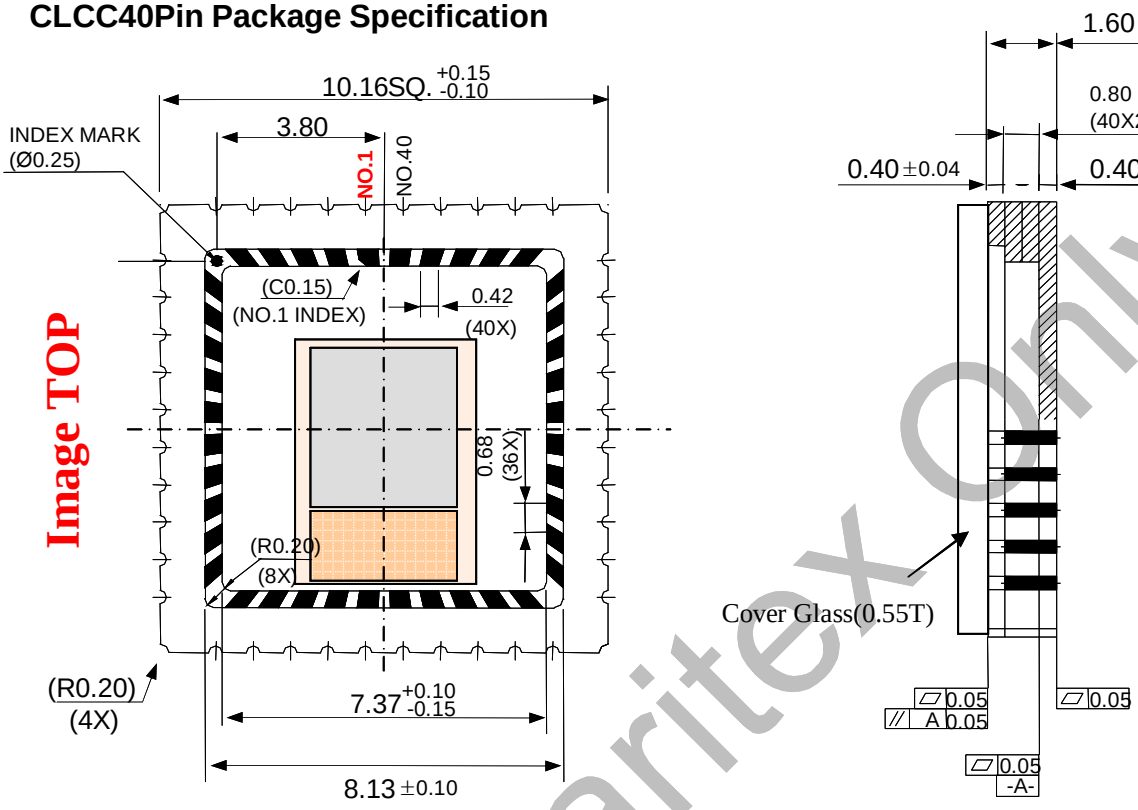
1) Measured sensitivity of Green pixel at 1.5lux illumination for 66ms integration time
Test area is the 128x96 of center area
2) For λ=550 wavelength
3) Measured at the zero illumination for 66ms at the 40 degree
(1) read the dark signal average of all pixels (640x480) for 66ms
(2) read the dark signal average of all pixels (640x480) for 0.132ms
(3) Dark signal @66ms(1)-Dark signal @0.132ms(2)
(4) convert to mV unit
4) For 16X12 pixel region under illumination with output signal equal to 50% of saturation signal. @128x96 of center area.

$$\frac{\text{Max value of Block} - \text{Min value of Block}}{\text{Average value of all blocks}} \times 100$$

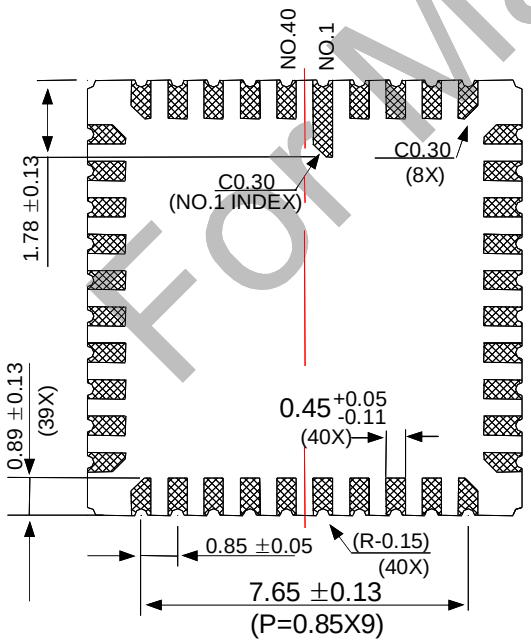
5) For frame rate = 15 fps
20*Log (Saturation Signal / Dark signal) [dB]

CMOS Image Sensor with 640 X 480 Pixel Array and Integrated On-Chip Image Signal Processor

CLCC40Pin Package Specification



Package center = Image area center



NOTE:
1. NI 2.0um + Au 0.5um MIN
2. NO METALLIZATION ON SEAL RING AND DIE ATTACH PAD.
3. UNIT : mm

CMOS Image Sensor with 640 X 480 Pixel Array and Integrated On-Chip Image Signal Processor

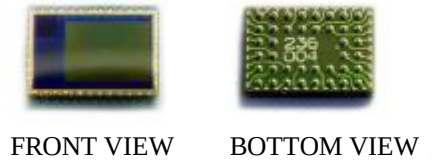
CSP(Chip Scale Package) Specification

	Symbol	Normal	Min	Max
Package Body Dimension X	**A**	3.830	3.805	3.855
Package Body Dimension Y	**B**	5.410	5.385	5.435
Package Height	**C**	0.970	0.900	1.020
Package Body Thickness	**C2**	0.840	0.795	0.865
Ball Height	**C1**	0.130	0.100	0.160
Ball Diameter	**D**	0.25	0.220	0.280
Pins Pitch X ,Y axis	**J**	0.68	.	.
Edge to Ball Center Distance along X	**S1**	0.555	0.525	0.585
Edge to Ball Center Distance along Y	**S2**	0.665	0.635	0.695

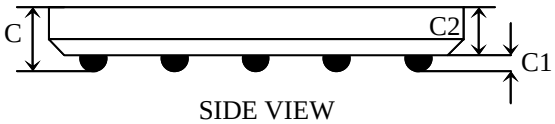
Table1. Package Dimensions Unit:mm

	1	2	3	4	5
A	PVDD	DVDD	FSYNC	PCLK	MCLK
B	DGND	PGND	HSYNC	SYNC DGND	DVDD
C	DVDD	NC		N.C	HVDD
D	D0	AVDD		STDBY	SCL
E	D1	D4		CREF_P	SDA
F	DVDD	D2	D6	RSTB	CREF_N
G	AGND	D3	D5	D7	AVDD

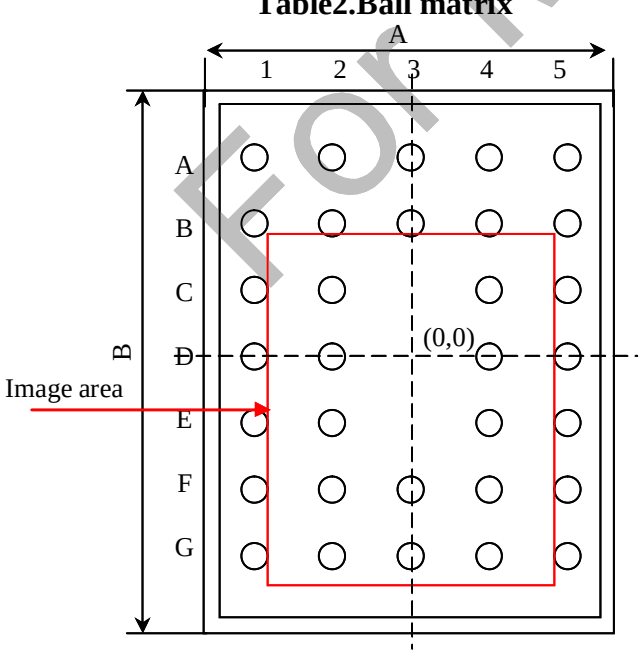
Table2.Ball matrix



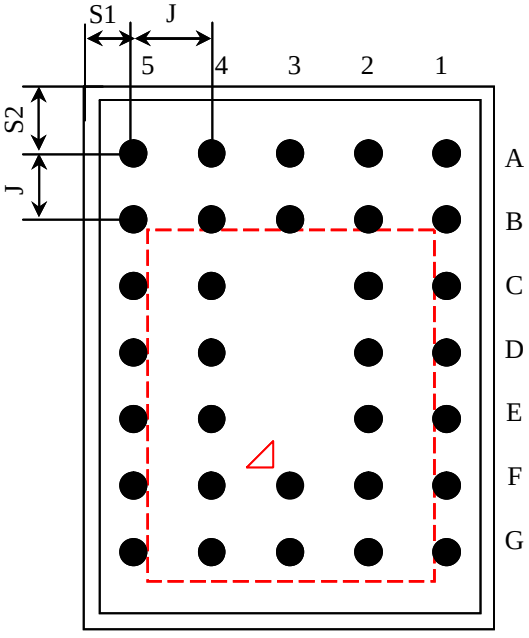
FRONT VIEW BOTTOM VIEW



SIDE VIEW



FRONT VIEW(Bumps DOWN)



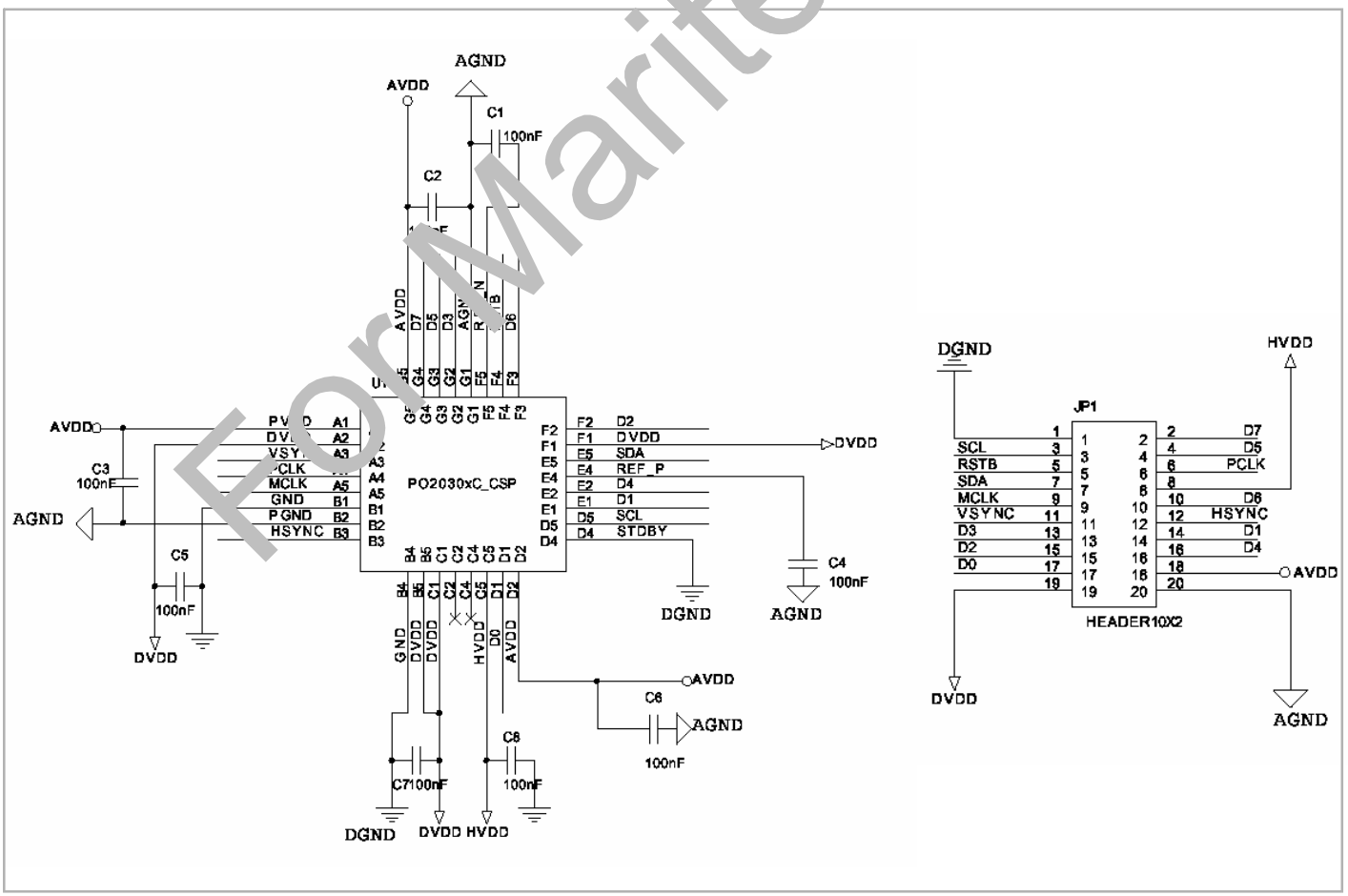
BOTTOM VIEW(Bumps UP)

CMOS Image Sensor with 640 X 480 Pixel Array and Integrated On-Chip Image Signal Processor

Module Specification(&Lens)

Module name	PO2030xC-MSx1-PP0x
Size	6.0mmX7.0mmX5.7(+0.0/-0.3)mm
Lens construction	2 Plastic & IR filter(0.4T)
Focal Length	3.37mm ± 5%
View angle	62.2º ± 5%(diagonal 4.16mm)
Aperture	F#2.8
TV Distortion	-0.94
Outer Mechanical Dimension is Flexible According to Customer's Requirement	

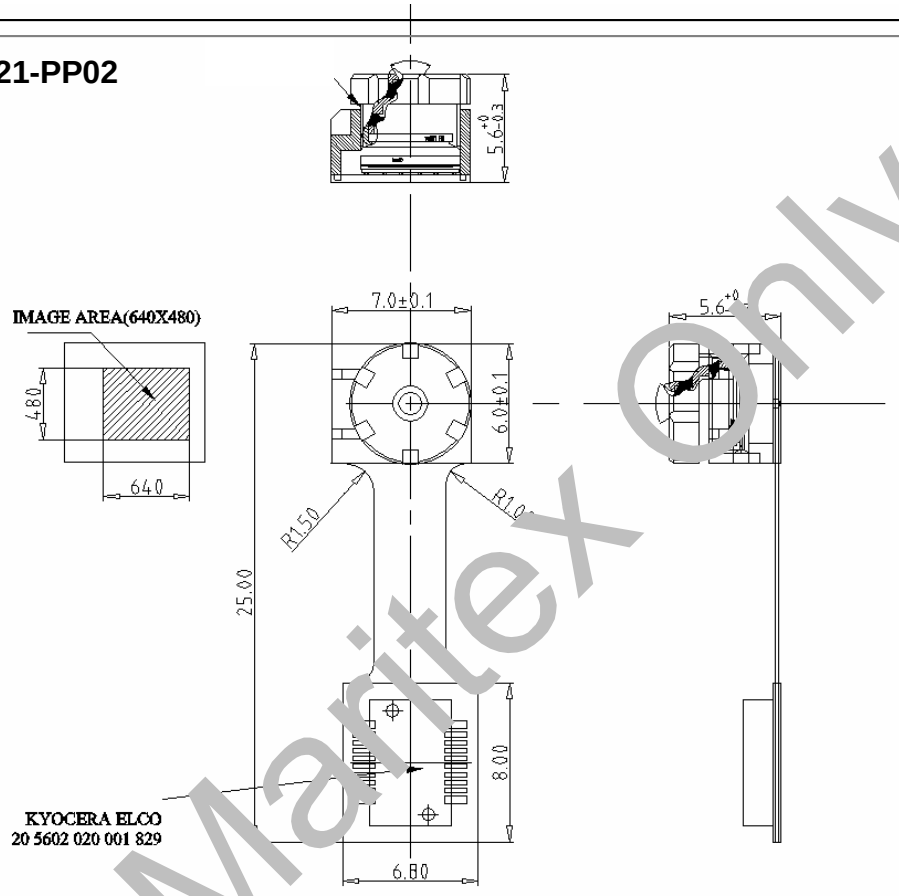
Module schematic for CSP



CMOS Image Sensor with 640 X 480 Pixel Array and Integrated On-Chip Image Signal Processor

Module Diagram (PIXELPLUS Standard Module)

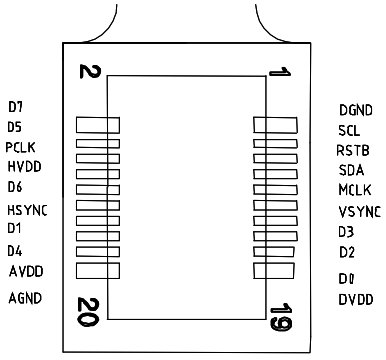
PO2030xC-MS21-PP02



Unit : mm

Standard Pin assignment

19	DVDD	20	AGND
17	D0	18	AVDD
15	D2	16	D4
13	D3	14	D1
11	VSYNC	12	HSYNC
9	MCLK	10	D6
7	SDA	8	HVDD
5	RSTB	6	PCLK
3	SCL	4	D5
1	DGND	2	D7



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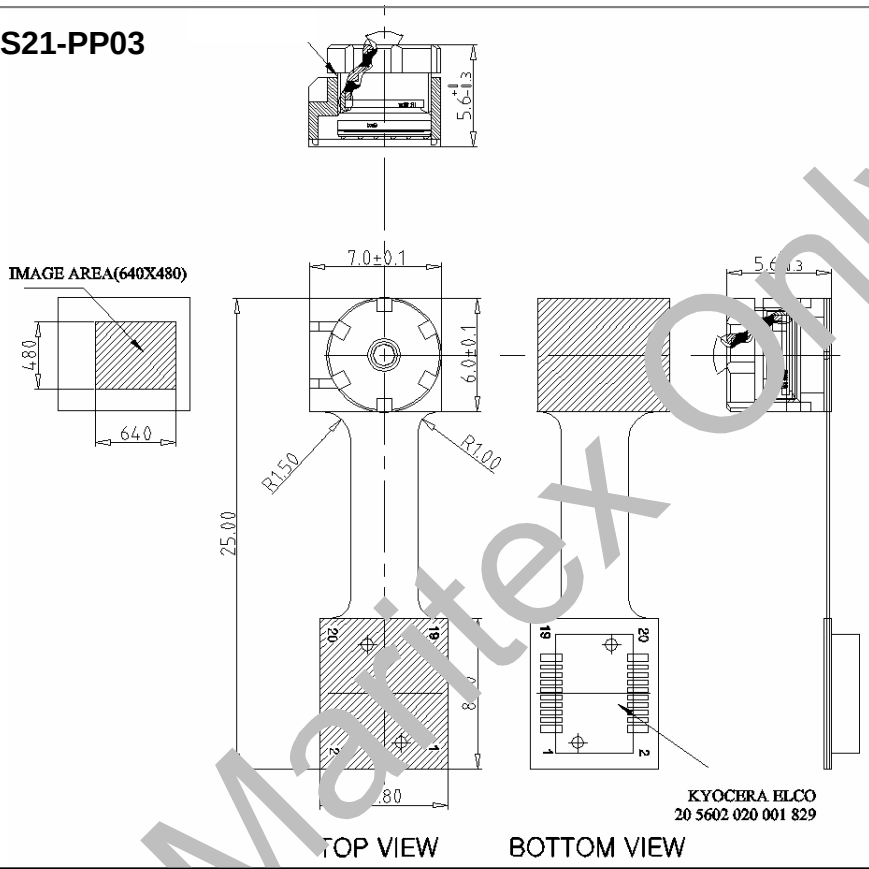
CMOS Image Sensor with 640 X 480 Pixel Array and Integrated On-Chip Image Signal Processor

Module Diagram

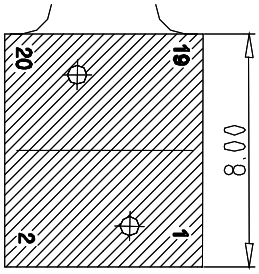
PO2030xC-MS21-PP03

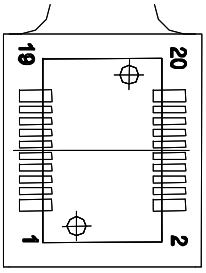


Unit : mm

Standard Pin assignment

19	DVDD	20	AGND
17	D0	18	AVDD
15	D2	16	D4
13	D3	14	D1
11	VSYNC	12	HSYNC
9	MCLK	10	D6
7	SDA	8	HVDD
5	RSTB	6	PCLK
3	SCL	4	D5
1	DGND	2	D7





Kyocera Elco Corporation
Socket Part No: 20 5602 001(000) 829

*Outer Mechanical Dimension is Flexible According to Customer's Requirement

APPLICATION NOTE

- Recommended Register Values (Write I2C Addr. : 0xDC, Read I2C Addr. : 0xDD)

Overview

- The better image can be acquired to set up recommended register value.

(1) Initial Setting

Reg. Addr. (Hex)	Recommended value (Hex)	Register Name	Default Value (Hex)	Descriptions
21	**00**	*Reserved*	21	
33	**36**	*Reserved*	3C	
36	**60**	*Reserved*	30	
37	**08**	*Reserved*	00	
3B	**31**	*Reserved*	33	
44	**0F**	*Reserved*	02	
50	**FC**	*ISPControl1*	FD	
51	**10**	*ISPControl2*	00	PCLK invert
58	**02**	*Reserved*	04	
66	**C0**	*Reserved*	E0	
67	**46**	*Reserved*	5F	
6B	**A0**	*Reserved*	E0	
6C	**34**	*Reserved*	5F	
7E	**25**	*CG11C (CbGain)*	20	1 ~ 254
7F	**25**	*CG22C (CrGain)*	20	1 ~ 254
8D	**0B**	*AutoControl*	03	2X weight window
92	**40**	*RefExp.*	38	
93	**04**	*MinGlbGain*	00	
94	**26**	*MaxGlbGain*	20	Max.Global Gain
95	**0A**	*AwbAeLock*	06	
99	**03**	*MaxExpTime(H0*	01	15 fps. -> 7.5 fps.
9A	**F0**	*MaxExpTime(L)*	F3	15 fps. -> 7.5 fps.
9D	**7A**	*AWBRed*	80	
C5	**02**	*Reserved*	00	
D6	**07**	*LensG*	00	

CMOS Image Sensor with 640 X 480 Pixel Array and Integrated On-Chip Image Signal Processor

Reg. Addr. (Hex)	Recommended value (Hex)	Register Name	Default Value (Hex)	Descriptions
59	**00**	*RGmmCoeff0*	00	R Gamma Coefficient
5A	**1A**	*RGmmCoeff1*	06	
5B	**2A**	*RGmmCoeff2*	0B	
5C	**37**	*RGmmCoeff3*	1E	
5D	**42**	*RGmmCoeff4*	31	
5E	**56**	*RGmmCoeff5*	49	
C8	**00**	*GGmmCoeff0*	00	G Gamma Coefficient
C9	**1A**	*GGmmCoeff1*	06	
CA	**2A**	*GGmmCoeff2*	0B	
CB	**37**	*GGmmCoeff3*	1E	
CC	**42**	*GGmmCoeff4*	31	
CD	**56**	*GGmmCoeff5*	49	
CE	**00**	*BGmmCoeff0*	00	B Gamma Coefficient
CF	**1A**	*BGmmCoeff1*	06	
D0	**2A**	*BGmmCoeff2*	0B	
D1	**37**	*BGmmCoeff3*	1E	
D2	**42**	*BGmmCoeff4*	31	
D3	**56**	*BGmmCoeff5*	49	
5F	**68**	*GmmCoeff6*	61	Common Gamma Coefficient
60	**87**	*GmmCoeff7*	84	
61	**A3**	*GmmCoeff8*	A2	
62	**BC**	*GmmCoeff9*	BD	
63	**D4**	*GmmCoeff10*	D8	
64	**EA**	*GmmCoeff11*	EC	

 # PO2030N will be set as follows by above recommended setting

- ***Max.Frame Rate : 15 fps. @ MCLK = 13.5 MHz, 30fps. @ MCLK = 27MHz***
- ***Auto Frame Rate Control : Min.Frame Rate = Max.Frame Rate / 2***
- ***Auto Gain Control : Max.Global Gain = 4X***
- ***Output Format : YUV422 (output range : 1 ~ 254)***
- ***Weight Window : 2X Center Weight***
- ***VSYNC (positive level), HSYNC (positive level), PCLK (positive edge)***
- ***Pixel Correction, Color Correction, Gamma Correction, AWB, AE***

(2) Additional setting according to the resolution

-VGA mode (640x480)

Reg. Addr. (Hex)	Recommended value (Hex)	Register Name	Default Value (Hex)	Descriptions
20	**44**	*Reserved*	44	

-QVGA mode (320x240)

20	**04**	*Reserved*	44	

-QQVGA mode (160x120)

20	**24**	*Reserved*	44	

- Max. frame rate and frequency in each mode

		VGA	QVGA	QQVGA
Bit 6 ~ 5 of Reg.20h		‘1x’	’00’	‘01’
Max. MCLK freq.		27 MHz	27 MHz	27 MHz
PCLK freq.	Bayer / Mono Output	13.5 MHz	6.75 MHz	3.375 MHz
	YCbCr Output	27 MHz	13.5 MHz	6.75 MHz
Image Size		640 x 480	320 x 240	160 x 120
Max. Frame Rate		30 fps.	30 fps.	30fps.

- Flicker Free Mode

Related Registers : Period50H (Reg.4Ch) ~ Period60L(Reg.4F), FdConrol (Reg.46h), AutoControl1 (Reg.8Dh)

(1) Manual Flicker Free Mode

Reg. Addr. (Hex)	Appropriate value (Hex)	Register Name	Default Value (Hex)	Descriptions
4C	Refer to following example	*Period50H*	00	
4D	,,	*Period50L*	B0	
4E	,,	*Period60H*	00	
4F	,,	*Period60L*	94	
9B	**14**	*Reserved*	10	

Reg. Addr. (Hex)	Flicker On (Hex)	Register Name	Flicker Off (Hex)	Descriptions
46	**20 / 40**	*FdControl*	00	60Hz / 50Hz
8D	**000xx1xx (b)**	*AutoControl1*	03	Flicker mode enable

-Flicker Period Control Register Setting

Related Registers **:** *Reg.4C(h), Reg.4D(h) – for 50Hz light source.*

Reg.4E(h), Reg.4F(h) – for 60Hz light source.

Flicker Period Reg. Value = 64*(MCLK Freq/(Frame Width * 2))/(Flicker Freq.*2)

ex) - 60Hz, MCLK = 13.5MHz

Frame Width = 900 column .

*Flicker Period = 64 * (13500000 / (900 * 2)) / (60 x 2) = 4000 = 0x0FA0*

Reg.4E(h) = 0x0F; Reg.4F(h) = 0xA0;

- 50Hz, MCLK = 13.5MHz

Frame Width = 900 column

*Flicker Period = 64 * (13500000 / (900 * 2)) / (50 x 2) = 4800 = 0x12C0*

Reg.4C(h) = 0x12; Reg.4D(h) = 0xC0;

(2) Auto Flicker Detection Mode

PO2030NC support auto flicker detection mode.

Reg. Addr. (Hex)	Appropriate value	Register Name	Default Value (Hex)	Descriptions
4B	(1.667ms * MCLK freq.) / 256	*Regclk*	2C	
4C	Refer to the example in the previous page.	*Period50H*	00	
4D	,,	*Period50L*	B0	
4E	,,	*Period60H*	00	
4F	,,	*Period60L*	94	
9B	**14**	*Reserved*	10	

Reg. Addr. (Hex)	Flicker On (Hex)	Register Name	Flicker Off (Hex)	Descriptions
46	**87**	*FdControl*	00	50Hz / 60Hz flicker Auto Detection
8D	**000xx1xx (b)**	*AutoControl*	000xx0xx (b)	

- Output Format

Related Registers : ISPControl2 (Reg.51h), Brightness (Reg.80h), Y Contrast (Reg.81h), CG11C (Reg.7Eh), CG22C (Reg.7Fh)

1) YCbCr422 (8 Bit, Y range : 16 ~ 235, Cb & Cr range : 16 ~ 240)

Reg. Addr. (Hex)	Setting value (Bin)	Register Name	Default Value (Hex)	Descriptions
51	**xxxx0000**	*ISPControl2*	00	Cb Y Cr Y…
	xxxx0001			Cr Y Cb Y…
	xxxx0010			Y Cb Y Cr…
	xxxx0011			Y Cr Y Cb…

Reg. Addr. (Hex)	Setting value (Hex)	Register Name	Default Value (Hex)	Descriptions
53	**08**	*ISPControl4*	28	
80	**10**	*Brightness*	00	
81	**80**	*Y Contrast*	94	
7E	**20**	*CG11C*	20	
7F	**20**	*CG22C*	20	

2) YUV422 (8 Bit, Y range : 1 ~ 254 , U & V range : 1 ~ 254)

Reg. Addr. (Hex)	Setting value (Bin)	Register Name	Default Value (Hex)	Descriptions
51	**xxxx0000**	*ISPControl2*	00	U Y V Y…
	xxxx0001			V Y U Y…
	xxxx0010			Y U Y V…
	xxxx0011			Y V Y U…

Reg. Addr. (Hex)	Setting value (Hex)	Register Name	Default Value (Hex)	Descriptions
53	**28**	*ISPControl4*	28	
80	**00**	*Brightness*	00	
81	**94**	*Y Contrast*	94	
7E	**25**	*CG11C*	20	
7F	**25**	*CG22C*	20	

3) RGB565 (8 Bit)

Reg. Addr. (Hex)	Setting value (Bin)	Register Name	Default Value (Hex)	Descriptions
51	**xxxx1000**	*ISPControl2*	00	R5G3, G3B5…
	xxxx1001			B5G3, G3R5…

4) RGB888 (12 Bit)

Reg. Addr. (Hex)	Setting value (Bin)	Register Name	Default Value (Hex)	Descriptions
51	**xxxx1010**	*ISPControl2*	00	R8G4, G4B8…
	xxxx1011			B8G4, G4R8…

5) RAW Bayer RGB (9 Bit)

Reg. Addr. (Hex)	Setting value (Bin)	Register Name	Default Value (Hex)	Descriptions
51	**xxxx0100**	*ISPControl2*	00	RGRG…GBGB…
	xxxx0101			GBGB…RGRG…
	xxxx0110			GRGR…BGBG…
	xxxx0111			BGBG…GRGR…

- Resolution : 642 x 482

Reg. Addr. (Hex)	Setting value (Hex)	Register Name	Default Value (Hex)	Descriptions
0B	**06**	*WindowY1 (L)*	08	642 x 482
0D	**52**	*WindowX2 (L)*	50	
2D	**43**	*Reserved*	41	
50	**A5**		FD	Color Correction Off
52	**x0xxxxxx (b)**	*ISPControl3*	x1xxxxxx (b)	
53	**2F**		28	Gamma Correction Off
79	**00**	*EdgeGain*	AC	Edge Enhancement Off

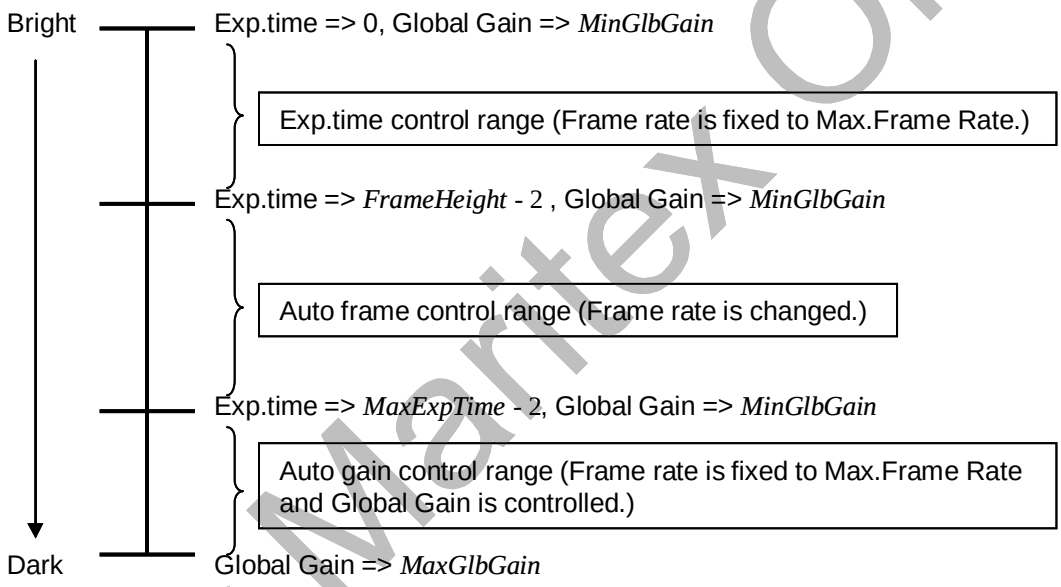
- Resolution : 644 x 484

Reg. Addr. (Hex)	Setting value (Hex)	Register Name	Default Value (Hex)	Descriptions
0B	**04**	*WindowY1 (L)*	08	644 x 484
0D	**54**	*WindowX2 (L)*	50	
29	**E8**	*Reserved*	E6	
2D	**45**	*Reserved*	41	
50	**A5**		FD	Color Correction Off
52	**x0xxxxxx (b)**	*ISPControl3*	x1xxxxxx (b)	
53	**2F**		28	Gamma Correction Off
79	**00**	*EdgeGain*	AC	Edge Enhancement Off

- AE Control

Related Registers : AutoControl1(Reg.8Dh), RefExpTime (Reg.92h), MaxExpTime (Reg.99h, 9Ah), MinGlbGain (Reg.93h), MaxGlbGain (Reg.94h)

If AE_EN of *Auto Control1(Reg.*8Dh) register is set to '1', *ExpTime*, *GlbGain* registers are automatically controlled by ISP to control overall brightness of sensor image. During auto exposure process, the brightness level of image is set by *RefExpTime* register. The average brightness of image is controlled to get close to *RefExpTime* register value with the margin set by *AWBAELock*[3:0] register. *ExpTime* register is controlled, at first. If integration line register are limited, frame rate controlled and then global gain register is controlled. Variation of *GlbGain* or *ExpTime* register are limited by *MinGlbGain*, *MaxGlbGain* and *MaxExpTime* registers, respectively.



1) Auto Frame Control

Auto Frame Control Method can be used to get brighter image in dark condition. Frame rate is automatically controlled by ISP between Max. frame rate and Min. frame rate.

Max. Frame Rate = (MCLK frequency) / (Frame Height * Frame Width * 2)
Min. Frame Rate = (MCLK frequency) / (*MaxExpTime* * Frame Width * 2)

Frame Height = *FrameHeight* (Reg.04h, 05h) + 1
Frame Width = *FrameWidth* (Reg.06h, 07h) + 1
Min. Frame Rate is controlled by *MaxExpTime* registers (Reg.99h, 9Ah) (*MaxExpTime* >= *FrameHeight*)

2) Auto Gain Control

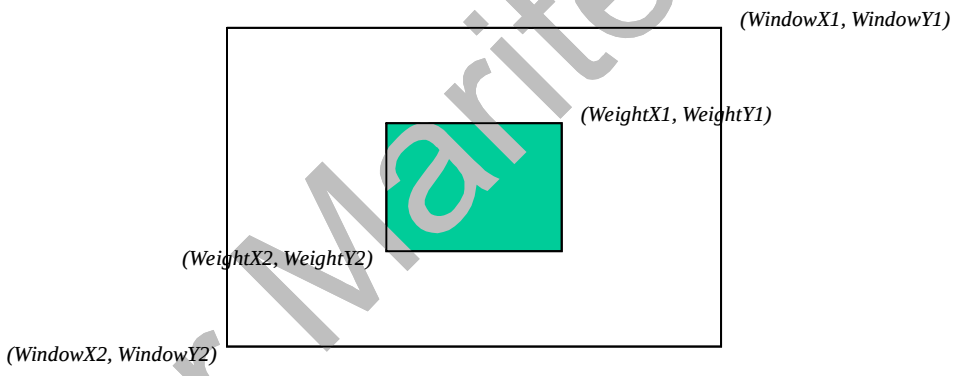
Auto Gain Control Method can be used to get brighter image in dark condition. Global gain is controlled automatically by ISP between *MaxGlbGain* (Reg.94h) and *MinGlbGain* (Reg.93h).

MaxGlbGain >= *MinGlbGain* (for *MinGlbGain,* follow our recommended value)

- Backlight Compensation

Related Registers : WeightX1(H) (Reg.A1h) ~ WeightY2(L) (Reg.A8h), AutoControl1 (Reg.8Dh), RefExpTime (Reg.92h)

Reg. Addr. (Hex)	Register Name	Default Value (Hex)	Description
A1	*WeightX1(H)*	01	**Minimum** : *WindowX1*(Reg.08h, 09h)
A2	*WeightX1(L)*	A5	
A3	*WeightX2(H)*	02	**Maximum** : *WindowX2*(Reg.0Ch, 0Dh)
A4	*WeightX2(L)*	7A	
A5	*WeightY1(H)*	00	**Minimum** : *WindowY1*(Reg.0Ah, 0Bh)
A6	*WeightY1(L)*	A7	
A7	*WeightY2(H)*	01	**Maximum**: *WindowY2*(Reg.0Eh, 0Fh)
A8	*WeightY2(L)*	47	



	Reg. Addr. (Hex)	Recommended Value (Hex)	Register Name	Default Value (Hex)	Description
1X Weight Compensation	8D	03	*AutoControl*	03	
	92	40	*RefExpTime*	40	
2X Weight Compensation	8D	0B			
	92	48			
4X Weight Compensation	8D	13			
	92	56			
8X Weight Compensation	8D	1B			
	92	72			

The target weight window size and position can be modified by ‘weight window register’. Please beware that weight window size has minimum and maximum value. You can choose weight of the compensation among 1x, 2x 4x and 8x , and you should choose the Y_target value which is related to weight.

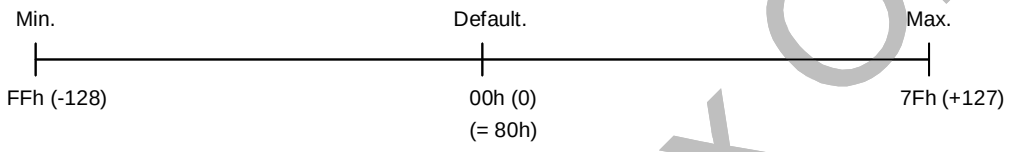
- Brightness / Y Contrast / Saturation / Color Rotation (Only for YCbCr422 & YUV422)

-Related Registers : Brightness (Reg.80h), Contrast (Reg.81h), CG11C (CbGain, Reg.7Eh), CG22C (CrGain, Reg.7Fh)

Y *reault* = Y * (Ycontrast / 128) + Ybrightness
Cb *result* = Cb * *CbGain* / 32
Cr *result* = Cr * *CrGain* / 32

(1) Brightness

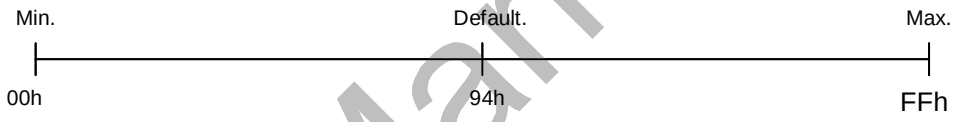
Brightness is controlled by *Brightness* register (Reg.80h). The default value of this register is 00h.



* Brightness(80h) : (bit7) | (bit6 ~ bit0) = sign digit | magnitude

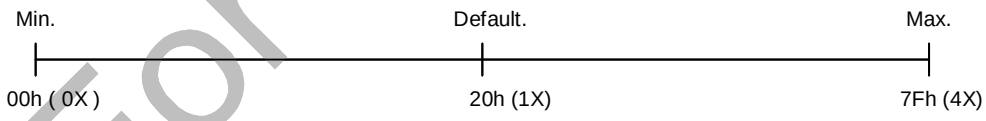
(2) Y Contrast

Contrast is controlled by Y *Contrast* register (Reg.81h). The default value of this register is 40h.



(3) Saturation

Saturation is controlled by *CG11C (CbGain)* and *CG22C (CrGain)* registers (Reg.7Eh, 7Fh) with the same values. The default value of these registers are 20h and these are controllable separately for adjusting color tone.



(4) Rotation

Color Rotation is controlled by *CG11C, CG22C, CG12C* and *CD21C* registers (Reg.7Eh, 7Fh, 80h and 81h) with the same values.

$$\begin{bmatrix} Cb\ result \\ Cr\ result \end{bmatrix} = \begin{bmatrix} cos\theta & -sin\theta \\ sin\theta & cos\theta \end{bmatrix} * \begin{bmatrix} Cb \\ Cr \end{bmatrix} = \begin{bmatrix} CG11C & CG12C \\ CG21C & CG22C \end{bmatrix} * \begin{bmatrix} Cb \\ Cr \end{bmatrix}$$

* Brightness(80h) : (bit7) | (bit6 ~ bit5) | (bit4 ~ bit0) = sign digit | integer | fractional

- Y target Control

Related Registers : RefExpTime (Reg.92h)

Y target is controlled by *RefExpTime* register (Reg.92h). The default value of this register is 40h.

<Ex.>

Level	0	1	2	3	4	5 (default)	6	7	8	9	10
Value (Hex)	18	20	28	30	38	40	48	50	58	60	68

- Color Correction Matrix

Related Registers : ColorMatrix11 (Reg.6Fh) ~ ColorMatrix33 (Reg.77h)

Color correction can be accomplished by color transform registers (Reg.6Fh ~ 77h) by means of the following equation, where ***CC*** is 3x3 color correction matrix.

$$\begin{pmatrix} CT0 & CT1 & CT2 \\ CT3 & CT4 & CT5 \\ CT6 & CT7 & CT8 \end{pmatrix} = \begin{pmatrix} m00 & m01 & m02 \\ m10 & m11 & m12 \\ m20 & m21 & m22 \end{pmatrix} = 32 * CC$$

* m00 ~ m22 : (bit7) | (bit6 ~ bit0) = sign digit | magnitude

<Ex.>

$$\begin{pmatrix} m00 & m01 & m02 \\ m10 & m11 & m12 \\ m20 & m21 & m22 \end{pmatrix} = 32 * \begin{pmatrix} 0.7396 & -1.1444 & 0.4048 \\ -0.6039 & 1.4137 & 0.1902 \\ -0.1025 & -1.3094 & 2.4119 \end{pmatrix} = \begin{pmatrix} 38h & A5h & 0Dh \\ 93h & 2Dh & 06h \\ 83h & AAh & 4Dh \end{pmatrix}$$

- Sharpness Control

Related Registers : EdgeFactor (Reg.79h), EdgeThreshold (Reg.7Bh)

Sharpness is controlled by *EdgeFactor1* register (Reg.79h) and *EdgeThreshold* register (Reg.7Bh). All three values have the following Min. and Max. value.

00h ≤ *EdgeFactor* ≤ 1Fh
00h ≤ *EdgeThreshold* ≤ FFh

The lowest sharpness level can be gotten by setting registers as follows.

EdgeFactor = 00h, *EdgeThreshold* = FFh

And, the highest sharpness level can be gotten by setting registers as follows.

EdgeFactor = 1Fh, *EdgeThreshold* = 00h

But, we recommend to set *EdgeThreshold* register value greater than 01h.

Ex.)

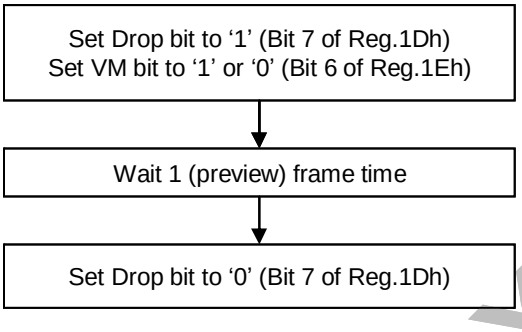
Sharpness Level	Reg. Addr. (Hex)	Recommended value	Register Name	Default Value
0	79	**xxx00000 (b)**	*EdgeFactor1*	xxx01100 (b)
	7B	**02 (h)**	*EdgeThreshold*	02 (h)
1	79	**xxx00110 (b)**		
	7B	**02 (h)**		
2	79	**xxx01100 (b)**		
	7B	**02 (h)**		
3	79	**xxx10010 (b)**		
	7B	**02 (h)**		
4	79	**xxx11000 (b)**		
	7B	**02 (h)**		
5	79	**xxx11111 (b)**		
	7B	**02 (h)**		

- Vertical / Horizontal Mirror

Related Registers : TgControl1(Reg.1Dh), TgControl2(Reg.1Eh)

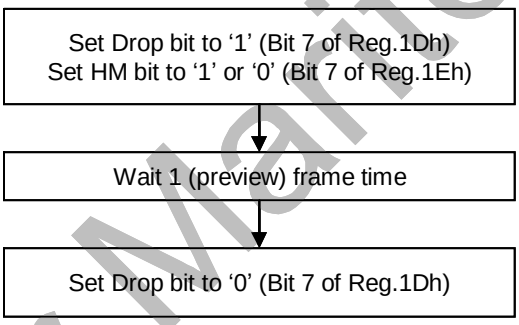
(1) Vertical Mirror

Vertical Mirror is controlled by VM bit (Bit 6 of Reg.1Eh)..



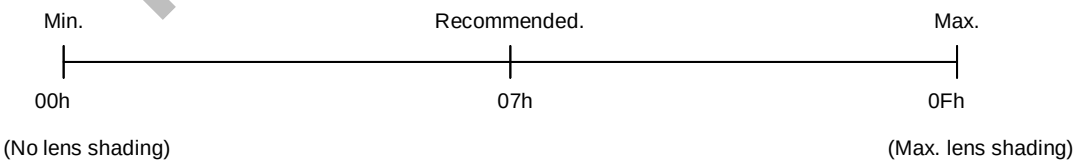
(2) Horizontal Mirror

Horizontal Mirror is controlled by HM bit (Bit 7 of Reg.1Eh).



- Lens shading

Related Registers : LensG(Reg.D6h),



- PC Board Layout Considerations

It is important that care be given to the PC board layout to reduce power noise. Figure 1 shows a recommended connection diagram for the PO2030.

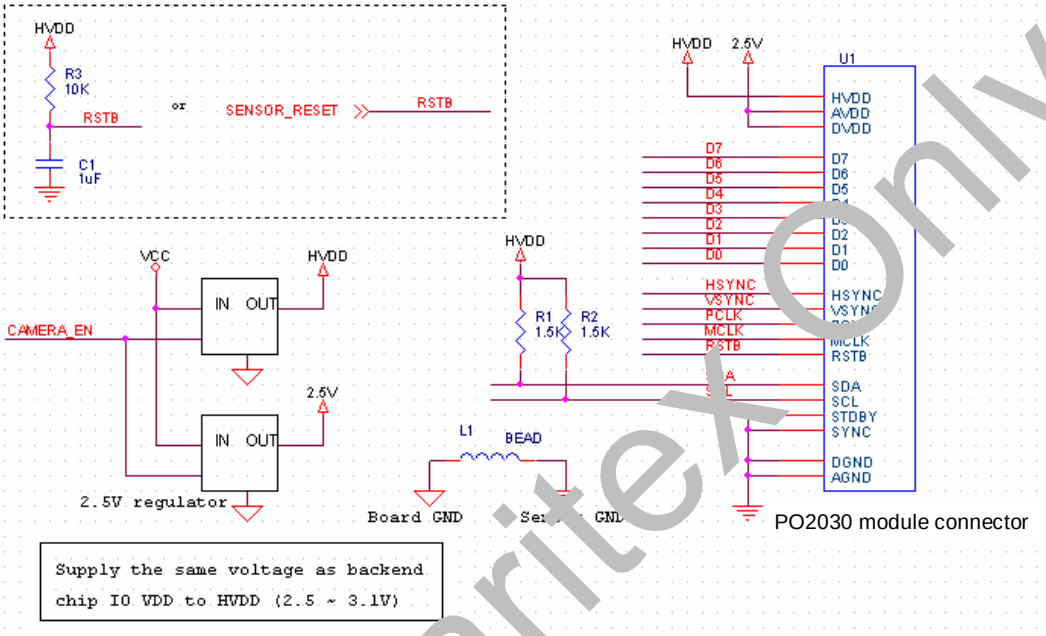


Figure 1. PO2030xC module typical connection diagram

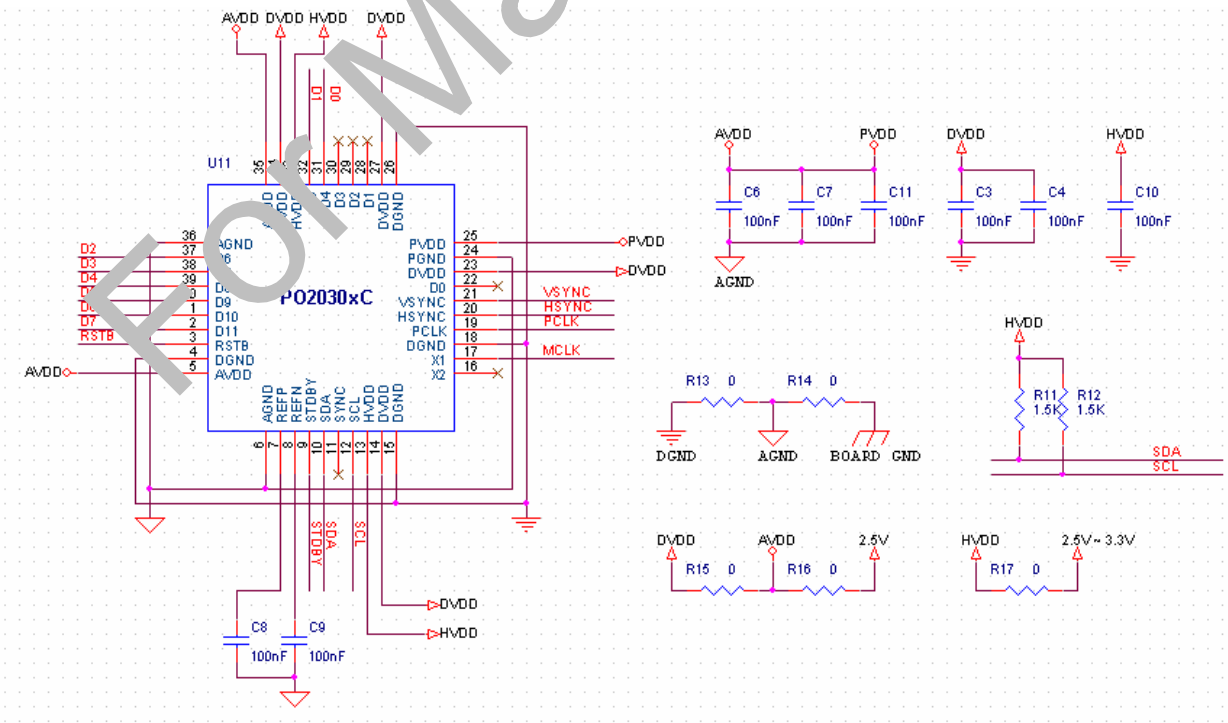


Figure 2. PO2030xC CLCC typical connection diagram

Ground Planes

The ground plain should connect to the regular PCB ground plane at a single point

Power Planes

The PC board layout should have the distinct power plane for PO2030xC. This power plane should have the separate regulator or be connected to the regular PCB power plane(VCC) at a single point through a ferrite bead, as illustrated in Figure 2. This power plane also has two distinct power planes, one for analog pins and one for digital pins. The analog power plane should encompass AVDD and PVDD pins, and the digital power plane should encompass DVDD pin.

Supply Decoupling

Noise on the PO2130xC power plane can be reduced by the use of multiple decoupling capacitors. (See Figure 2.) Optimum performance is achieved by the use of 0.1uF ceramic capacitors. Each of the power pins should be individually decoupled to ground. This should be done by placing the capacitors as close as possible to power pins with the capacitor leads as short as possible, thus minimizing lead inductance.

- Stand-by method

Method 1. Power cut-off

⇒ You can control stand-by mode by power control.
(Refer to Figure 1 : CAMERA_EN signal can be controlled by Backend chip or MCU.)

⇒ ***STDBY pin must be connected to '0'(DGND).***

⇒ ***Sensor reset can be auto-controlled by connecting RSTB pin to HVDD not other VDD using 10K resister and 1uF capacitor as shown in Figure 1.***

Method 2. Standby pin

⇒ You can control stand-by mode by using STDBY pin.

⇒ **MCLK must be fixed to '1' or '0' after STDBY pin is set to '1' to avoid the leakage current.**

'0' : normal mode
'1' : stand-by (sleep) mode

Method 3. I2C Stand-by

⇒ You can control stand-by mode by setting STDBY bit (bit 6) of Reg.1Fh.

⇒ **MCLK must be fixed to '1' or '0' after STDBY bit is set to '1' to avoid the leakage current.**

⇒ ***STDBY pin must be connected to '0'(DGND).***

'0' : normal mode
'1' : stand-by (sleep) mode